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A DSP SYSTEM FOR GENERIC POWER CONTROL APPLICATIONS

J. A. Restrepo(1), A. Cabello(2), J.M. Aller(1), M.I. Giménez de Guzmán(1), V. M. Guzmán(1) and A. Bueno(1)

(1) Universidad Simón Bolívar, Venezuela (2) UNEXPO, Venezuela

ABSTRACT

This work presents the development of a generic platform using a DSP as the processing unit, for testing control algorithms on switched based power systems. The aim of this project is to develop the control algorithms in a personal computer and to perform the actual task on an independent processor, allowing the personal computer to perform a man machine interface. The experiments show the adaptability of the platform for performing different control strategies commonly found in power electronics applications (scalar, vector and direct torque control strategies, neural network and parametric estimation, etc.).

INTRODUCTION

A DSP based platform has been developed for the implementation of AC machine control algorithms. The processing requirement for sophisticate control algorithms, such as vector control, calls for the use of special processing units. The present work focuses specially on the platform's computational unit. The use of microprocessors for the control of AC machines started in the early 80's [1], and now they play an important role in defining the system capabilities. Since the control strategies for a digital based system is best described in the discrete time-amplitude domain, a special set of mathematics has to be used to describe the system's dynamics [2]. In this case the DSP has a processing advantage over conventional microprocessor. The DSP internal architecture has been optimised for performing tasks commonly found in signal processing algorithms [3].

For the present work a floating point DSP AD-21061 was used as the main processing unit. The design of the processing unit has been done considering its future use as a teaching workbench [4]. This requires a careful design of the communications interface, making this as friendly as possible. With this purpose in mind a virtual instrument, using Lab-Windows CVI, was implemented for program downloading and information gathering between the DSP board and the personal computer.

Scalar, vector and direct torque control strategies had been tested, showing the system performance and adaptability. The developed system has proved its usefulness in undergraduate and graduate teaching courses as well as research activities.

PROCESSING AND ADQUISITION SUBSYTEMS

A diagram of the test rig is shown in Fig.1 and a picture of the implemented system in Fig. 3. The three-phase AC motor has coupled to its shaft a dynamic load implemented with a DC motor. For some applications a speed measurement is required, and this is performed with a 1000 pulses per cycle optical-encoder. Stator current in two of the three motor phases, as well as voltage and current in the DC bus link are measured using Hall effect sensors with the analogue output connected to the acquisition module. Those measurements and the switching state information are used for describing stator voltage and current space vectors. The DSP processing unit used in this work was an EZ-KIT evaluation unit for the SHARC DSP processor (AD-21061). This card was connected to the PC through the serial port. The connection between this card and the inverter system was performed through a specially designed extension card described below, allowing control over the switching elements, directly from a digital port or from the PWM unit. The EZ-KIT card has a monitoring programme for exchanging data with the PC, but on the PC side a library of functions was developed for communicating the personal computer with de DSP board.

Expansion card

The expansion card, shown in Fig.2 was design to complement the DSP card with the motor control tasks. A motion coprocessor ADMC-201 performs most of the power related tasks [5], and is used to reduce the components count number in the interface card.

The motion coprocessor is composed of several blocks. Among them, the vector transformation block performs the forward and reverse Clark and Park transformations. The PWM timer block performs several of the tasks involved in the generation of pulses for the voltage source inverter. The analogue to digital block consists of an 11-bits A/D converter, feed from four simultaneously sampled inputs, and a four-multiplexed channels extension. Finally, this coprocessor includes a six bits fully programmable I/O.

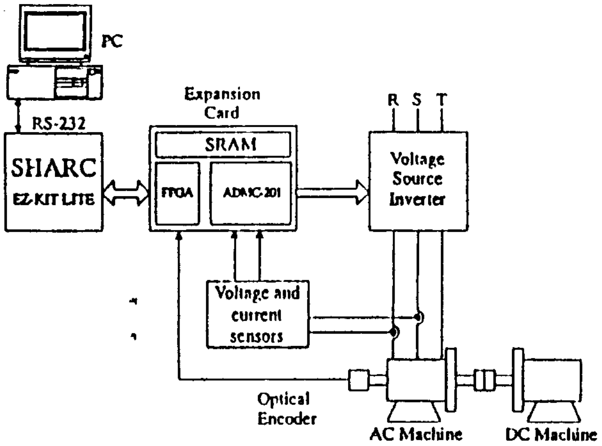

Figure 1. Test rig diagram for the DSP based system.

A FPGA was used for mapping in memory space the different devices in the extension card, and also for implementing a digital tachometer, included for machine control. This digital tachometer was implemented using a 24 bits binary counter clocked with a 40Mhz clock.

THE INTERFACE PROGRAM

As mentioned before, the PC is used for developing dc control software to be used by the DSP based system, and for supervising the system during normal operation. The DSP board contains a communications kernel for transferring and receiving information from the PC.

The structure of the programme environment is as follows, from the highest level in the PC to the lowest level in the DSP.

Virtual instrument implemented using the Lab-Windows CVI programming environment. It allows the user to visualise in real time, and to change the value of the different control variables. A graphic interface shows the user the control algorithm being executed by the DSP. It also allows the downloading to disk of the different variables. The main tasks of the supervisory system are:

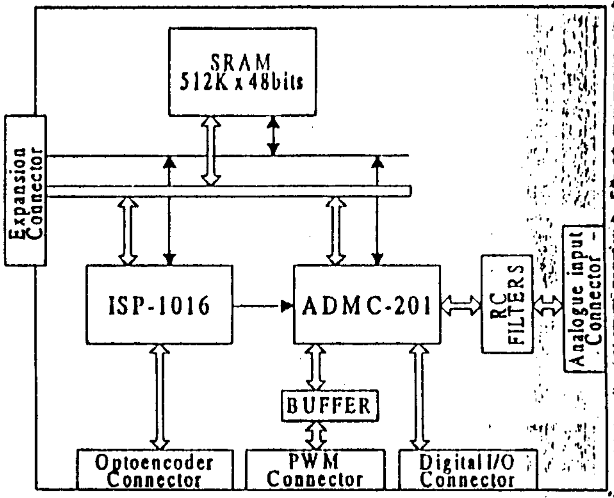

Figure 2. DSP extension card block diagram.

- Man machine interface.
- Downloading of the control algorithms to the DSP board.
- To start and stop the AC machine.
- Gathering and control of the machine speed.
- Visualise and saving to disk of the different control variables.

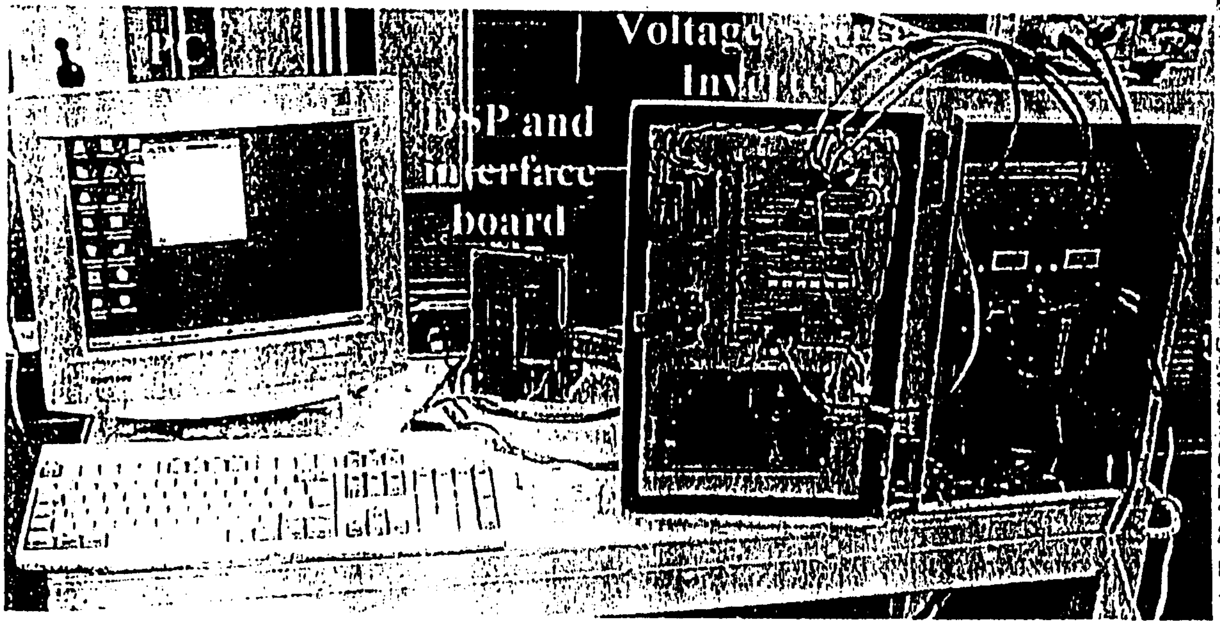

Figure 3. Actual test rig

Figures 4 and 5 show two examples of the program interface for scalar and space vector controllers respectively.

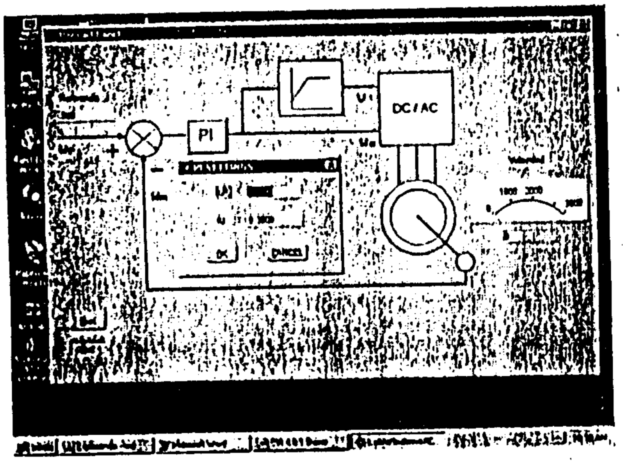

Figure 4. Scalar controller windows interface

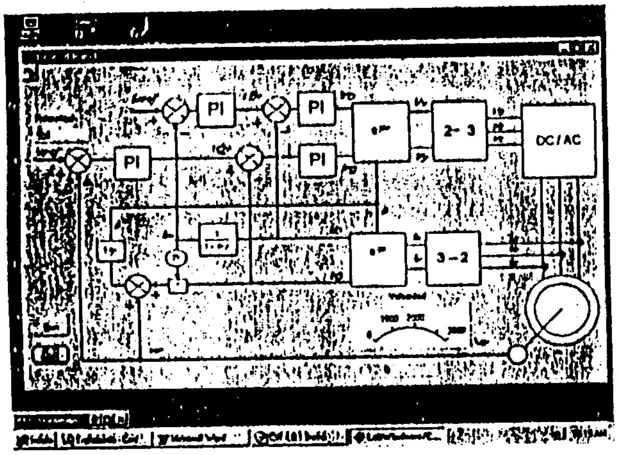

Figure 5. Space vector controller windows interface

EXPERIMENTAL TESTS

Some typical control algorithms, from standard scalar forms to the more complex vector control were employed for testing the DSP based platform. Figure 6 shows a phase stator current during the machine's star up, using a space vector control algorithm. Figures 7 and 8 shows the speed evolution over time for a ramp and step speed reference respectively, when a vector control is used. During the implementation of the test the versatility of the interface was tested, using different kind of controller parameters, changed on line with the operation of the system. Figure 9 illustrates the space vector trajectory for the stator current during steady state operation with nominal load.

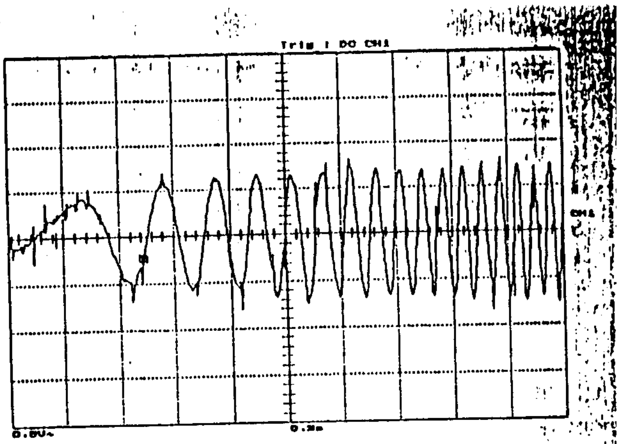

Figure 6. Stator current during the start up with space vector controller (Oscillogram)

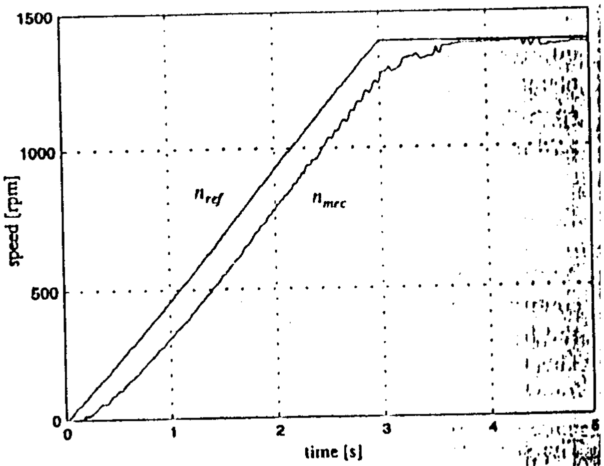

Figure 7. Ramp speed response using space vector controller

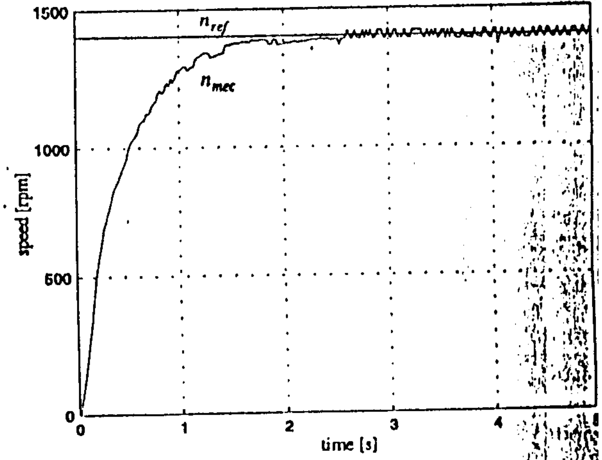

Figure 8. Step speed response using space vector controller

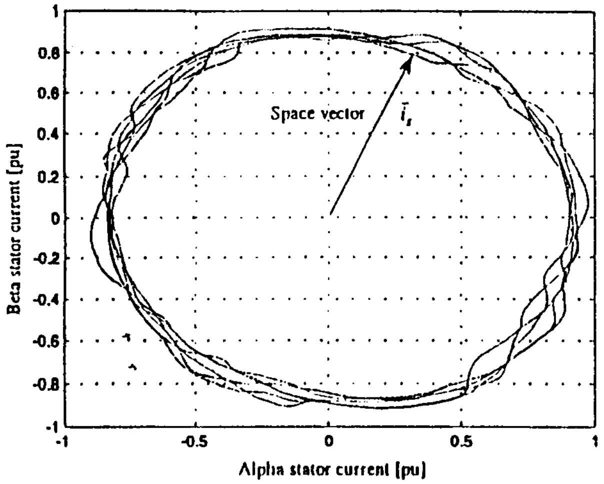

Figure 9. Stator current space vector in load condition

Results show the that all the tested algorithms require little programming effort, thanks to the use of high level programming language. The graphical interface also saves time for doing on-line modifications on the controller parameters, also the results were represented by charts to illustrate the systems response. The results also show that the resolution used by the motion co-processor, in the acquisition and transformation blocks, is enough for performing the control task. The chosen DSP didn't require additional memory for performing the vector control algorithm, saving money and space in the final implementation of the interface card.

CONCLUSIONS

In this work a generic platform for power electronics applications has been developed and tested using standard scalar and space vector control strategies. The controller was programmed for a graphical interface using Lab Windows CVI and C++ language. An extension board was developed for interconnecting an EZ-KIT evaluation unit, for the SHARC DSP processor (AD-21061), with the voltage source inverter. Each block in the interface card was tested individually, ranging from each sub-system in the motion co-processor (A/D conversion, vector transformation block, PWM block and digital I/O port), as well as the digital counter for measuring the machine's speed programmed in the FPGA.

The developed system is economic, flexible and can be easily adapted to new control algorithms. Also, is useful in training undergraduate and graduate electrical engineering students, as well as for research activities.

The chosen DSP allows for fast execution of the control algorithms.

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AUTHOR'S ADDRESS

The first author can be contacted at:

Universidad Simón Bolívar, Valle de Sartenejas, Baruta,
Edo. Miranda, Caracas 1080-A, Venzuela.
email: restrepo@usb.ve