Design of current control loop for grid connected inverters operating under nonideal grid conditions

Julio Viola *†, José Restrepo ‡, José Manuel Aller †‡, Flavio Quizhpi *, and Marco Fajardo *
* Universidad Politécnica Salesiana
Cuenca, Ecuador, EC010105
Email: jcviola@ieee.org
† SENESCYT - Prometeo Project, Ecuador
‡ Universidad Simón Bolívar, Caracas, Venezuela, 1080A

***Abstract*—A case study for designing the current control loop for single-phase inverters connected to weak grids is presented. The problems associated to the design of current control loop when highly distorted grid voltages are present and LCL filters are used to couple the inverters to the grid, are analyzed. Fourier coefficients decomposition is used to obtain an ahead-of-time version for the nonideal voltage signal which allows to compensate the current control loop delay. Also the relevance of a nonideal characteristic of the inverter as the dead-time effect on the shape of the controlled current is analyzed and compensated.**

***Index Terms*—power grids; pulse width modulation inverters; fourier series; current control;**

I. Introduction

The design of grid connected inverters (GCI) involves many challenges imposed by the tight requirements of different standards (notably IEEE 1547 [1] and IEC 61727 [2]). High quality for the injected current, islanding condition detection, low voltage ride-through capabilities (LVRT), and maximum power point tracking (MPPT) are just some of the most relevant. Economic reasons lead the designers to adopt the use of more compact filters to couple the inverter to the grid. The preferred topology is the LCL filter which offers better attenuation of switching harmonics than the purely inductive filter. Moreover its construction cost is lower and more compact since the values of required inductances are about one order of magnitude smaller than the purely inductive filter. Also by using less copper in the windings, Joule effect losses are reduced [3]. The use of LCL filters, however, carries two main disadvantages: the phenomenon of resonance which leads to undesirable peaks of current, and the increased sensitivity of the current to mismatches in the control voltage applied by the inverter. The first problem can be solved with an appropriate selection of inductances and capacitance values, so that the resonance frequency lies in a void zone of the spectrum, between the switching frequency harmonics and the higher expected grid frequency harmonics. The problem of the sensitivity is more complex to address since it depends on several nonideal characteristics of the pulse width modulated voltage source inverters (PWM-VSI), namely: discrete nature of the voltage steps imposed by the PWM, the need of setting dead-times between the turn on and turn off signals, and the delay in the computation of the control action associated to the digital loop. Regarding the grid conditions, an additional nonideal characteristic is the total harmonic distortion (THD) of the grid voltage. In the case study presented in this work a line with more than 7% of grid voltage THD is used in the simulations and in the experimental tests. This level of THD is not uncommon in some electric systems, especially in rural areas where weak line voltage profiles are highly affected by any nonlinear load [4]. The present paper covers the design considerations to deal with a current control loop in a GCI operating in a grid with high voltage THD, considering also the impact in the current shape due to dead-times and how to overcome this problem. It is shown that nonideal characteristics of the inverter make the control of sinusoidal currents with small amplitudes more complicated than those with higher amplitudes. A mixed solution by using a proportional-integral controller and a predictive scheme is proposed. Also the problem of digital control loop delay compensation is addressed and a technique based on a Fourier coefficient expansion is presented.

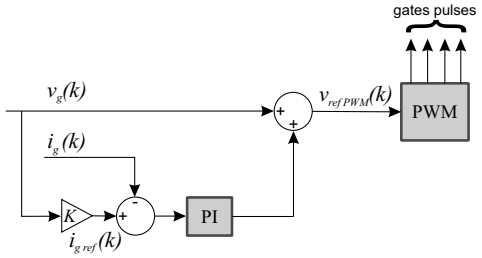


Figure 1: Proportional-integrative controller with feedforward of grid voltage.

II. Current loop design

Classic proportional-integral (PI) controller produces good results for current loops in GCI if appropriate considerations are taken into account in its design, namely transformation of ac quantities to a d-q rotating reference frame so the PI have to track dc quantities which greatly improves its performance. An alternative to variable transformation is to use feedforward of the grid voltage signal adding it to the controller's output [5]. Fig. 1 shows the blocks diagram for the PI scheme with feedforwarded grid voltage. Both techniques allow to obtain an

978-1-5090-2039-3/16 $31.00 © 2016 IEEE
DOI 10.1109/GreenTech.2016.13

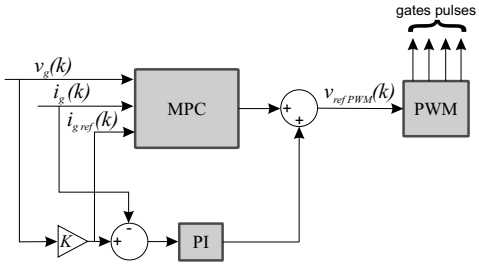


Figure 2: Hybrid control scheme with MPC and PI actions.

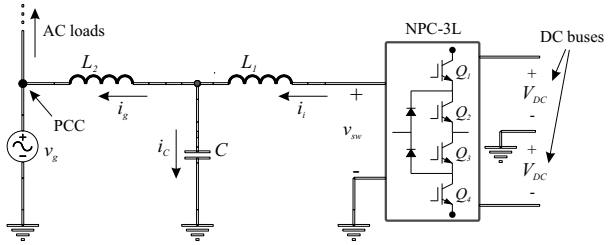


Figure 3: One-phase three-level neutral point clamped grid connected inverter.

acceptable tracking of the current reference if the grid voltage has a low THD and the amplitude of the current reference is relatively high. For those cases when highly distorted grid voltages are present or grid currents with small amplitudes have to be generated, the PI performance quickly degrades. For those controllers based on the transformation of variables to a d-q reference frame, the THD of the grid voltage lead to transformed voltages that are not longer dc quantities and the performance is degraded if corrections in the design are not implemented [6] [7]. These effects are more noticeable if LCL filters are used since the lower values typically used for the inductances increase the sensitivity of the control loop.

A. Hybrid predictive scheme

Model predictive control (MPC) is widely developed for inverters connected by means of purely inductive filters [8], [9]. A lesser number of papers can be found for MPC applied to GCI with LCL filters [10]. In [11] the authors proposed a discrete expression which can be used in the current loop to obtain the value of converter's voltage to be synthesized so the current error is reduced to zero. An inherent disadvantage of MPC schemes is the dependence of parameters values used in the predictive model. For a GCI with LCL filter, the uncertainties in the values of both inductors and the capacitor may lead to tracking errors in the sinusoidal current injected to the grid. In this paper a PI action is added to the output of the MPC so the tracking errors can be compensated. In Fig. 2 the proposed hybrid scheme is shown.

In this paper a 3-level neutral point clamped (3L-NPC) converter is used which is shown in Fig. 3. The classic pulse width modulation scheme for this type of inverter uses two 2-level (2L) modulators as shown in Fig. 5. The normalized modulating signal is shifted by 1 and introduced to the lower modulator which is in charge of generating the gate signals for Q_2 and Q_4, while the upper modulator generates the gates signals for Q_1 and Q_3.

B. Influence of delays

Delays are inevitable in digital control loops being mainly due to the time required to sample the electric variables used in the control algorithm and the time employed for the pulse width modulator to synthesize the inverter's output voltage. These delays can be neglected in most control schemes when the GCI uses purely inductive filters, but when LCL filters are used the control sensitivity is increased and the effect of the delays may degrade the control loop performance. In Figs. 1 and 2 the PI and hybrid control schemes use the grid voltage v_g to compose the control action. When a low distorted grid voltage is present, different versions of phase-locked loops (PLL) can be used to detect the voltage phase and, by adding a constant offset to the detected phase, an ahead-of-time version of the grid voltage can be obtained so the inherent delay of the digital control loop is compensated. For highly distorted grid voltages this method is not longer valid since the different harmonics present in the voltage have different phases. A decomposition by using Fourier series coefficients is proposed in this work. After the decomposition, the offset can be added to the different detected phases to reconstruct the ahead-of-time version of the distorted voltage. The resulting method is easier to implement than others proposed in the literature [12].

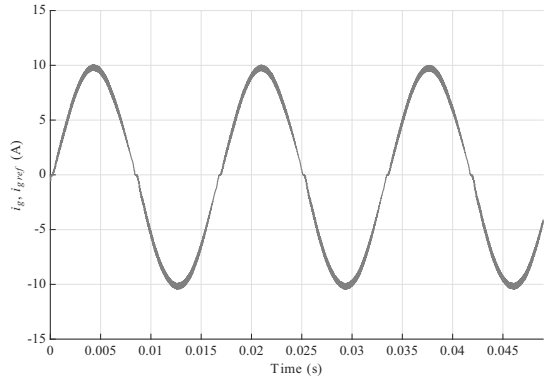
C. Influence of dead-times

Dead-times included between the rising and falling edges of gates signals have as final effect the reduction of the net voltage-seconds applied in the inverter's output. Their influence, however, in the shape of the current being controlled is totally different depending on the values of the inductors used in the coupling filter. For purely inductive filters the effect is almost unnoticeable if compared with the current spikes produced in the current when LCL filters are used. In Fig. 4 a comparison is shown for the current injected by an inverter operating with the same electrical conditions but using purely inductive filter in Fig. 4(a) and an LCL filter in Fig. 4(b). There are different approaches to cope with the effects that dead-times provoke in the current. These effects also depend on the power factor of the load connected to the inverter. In this paper a unity power factor operation is assumed and an offset is calculated and applied to the modulating signal sent to the pulse width modulator so the missing voltage-seconds are recovered. If $T_s = 1/f_s$ is the switching time, the ideal voltage-seconds applied by the inverter for a given duty cycle D are

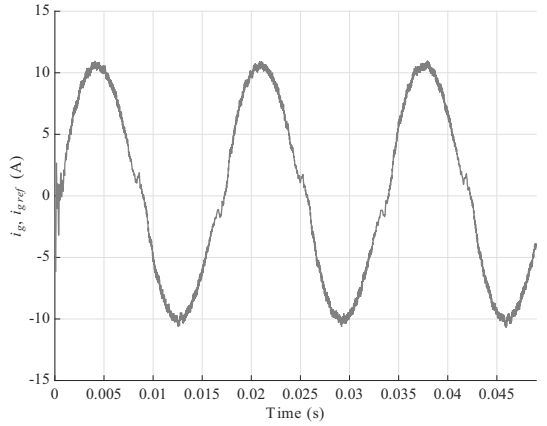
$$V.s_{ideal} = V_{DC}\, D\, T_s = V_{DC} \frac{t_{ON}}{T_s} T_s = V_{DC}\, t_{ON} \quad (1)$$

where V_{DC} is the DC bus voltage. If a dead-time t_{DT} is now considered between the turn off and the turn on of IGBTs, the applied voltage-seconds are

$$V.s_{real} = V_{DC} \frac{(t_{ON} - t_{DT})}{T_s} T_s = V_{DC}\, t_{ON} - V_{DC}\, t_{DT} \quad (2)$$



(a)



(b)

Figure 4: Grid currents for GCI coupled with (a) a purely inductive filter and (b) an LCL filter.

resulting in a reduction of the net voltage-seconds of $V_{DC}\, t_{DT}$. The compensation is implemented recalculating the modulating signal so that the voltage-seconds are again $V_{DC}\, t_{ON}$. The compensated duty cycle D_c will be

$$D_c = \frac{t_{ON} + t_{DT}}{T_s} \tag{3}$$

so that additional $V_{DC}\, t_{DT}$ volt-seconds are generated. In a practical manner the D_c is obtained by adding an offset to the normalized modulating signal v_{refPWM} that is sent to the pulse width modulator. The typical modulation scheme for a 3L-NPC inverter uses two standard 2-level pulse width modulators where the normalized voltage reference is shifted by 1 before being compared with the carrier of the second modulator. The scheme is shown in Fig. 5, and the corresponding compensated modulation scheme is shown in Fig. 6 where the offset $\frac{t_{DT}}{T_s}$ is added for the signal sent to the upper modulator and is subtracted for the signal sent to the lower one.

III. Simulations

Simulations in MATLAB/Simulink© are performed to show the effects of different nonidealities being considered in the design and how each problem is addressed. The simulated GCI has a nominal power of 5kW, the buses voltages are 250V and the switching frequency is 16kHz. The LCL filter has the following values: $L_1 = 760\mu$H, $L_2 = 40\mu$H and $C = 20\mu$F. The nominal grid voltage is 120Vrms but with the harmonic components shown in Table I.

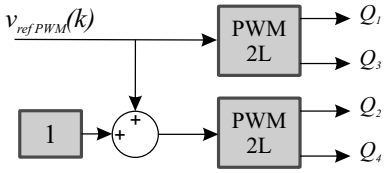


Figure 5: Pulse width modulator for the 3L-NPC.

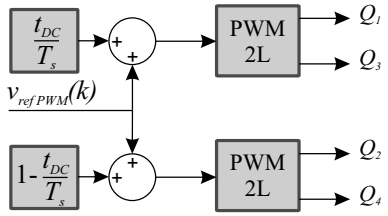


Figure 6: Pulse width modulator for the 3L-NPC with compensation of dead-times effect.

A. Operation with low amplitude currents

A PI controller tuned with a classic Ziegler-Nichols method is used to track the current reference and its performance is compared with the hybrid scheme proposed in this paper. A relatively high amplitude reference of 25A is set and the results are shown in Fig. 7(a) for the PI controller and in Fig. 7(b) for the hybrid controller. After a tuning of the PI proportional and integral gains a THD of 6% is obtained for the grid current while a 1% is obtained with the hybrid scheme. As a comparison a current reference with an amplitude of 2.5A is used and the results for both controllers are shown in Figs. 8(a) and 8(b). The improvement obtained with the hybrid controller is more evident for lower current amplitudes. In this example the current THD goes from 15% for the PI to 7% with the hybrid controller.

B. Operation with compensation of delays in feedforward grid voltage signal

The influence exerted by the delays associated to the feedforward signal is analysed. A simulation is run for a 10A current reference amplitude and from $t = 0$ to $t = 50ms$ the measured grid voltage is used as feedforward signal to calculate the control action. After $t = 50ms$ the reconstructed

Table I: Percentage harmonic contents for the simulated grid voltage

Harmonic order	% of the fundamental
3^{rd}	5
5^{th}	3
7^{th}	1.5
9^{th}	0.5

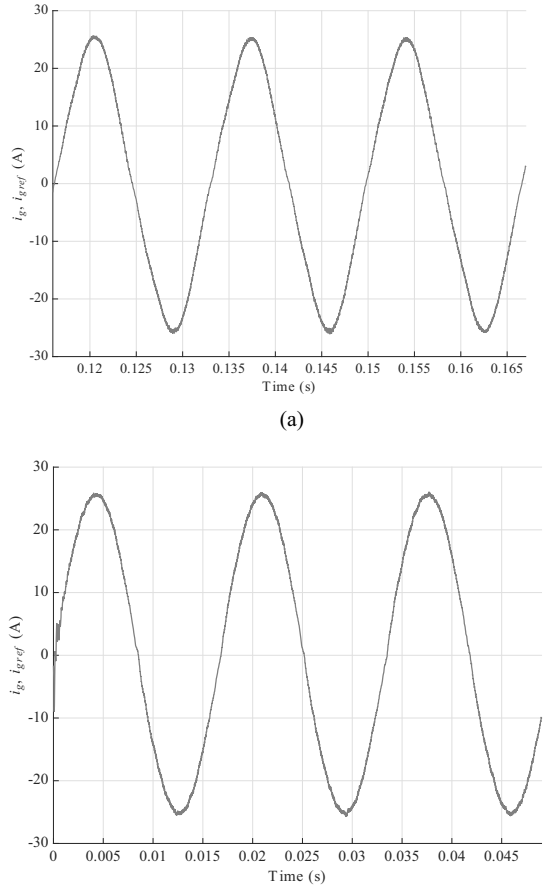


Figure 7: Grid current obtained for (a) the PI controller and (b) the hybrid controller.

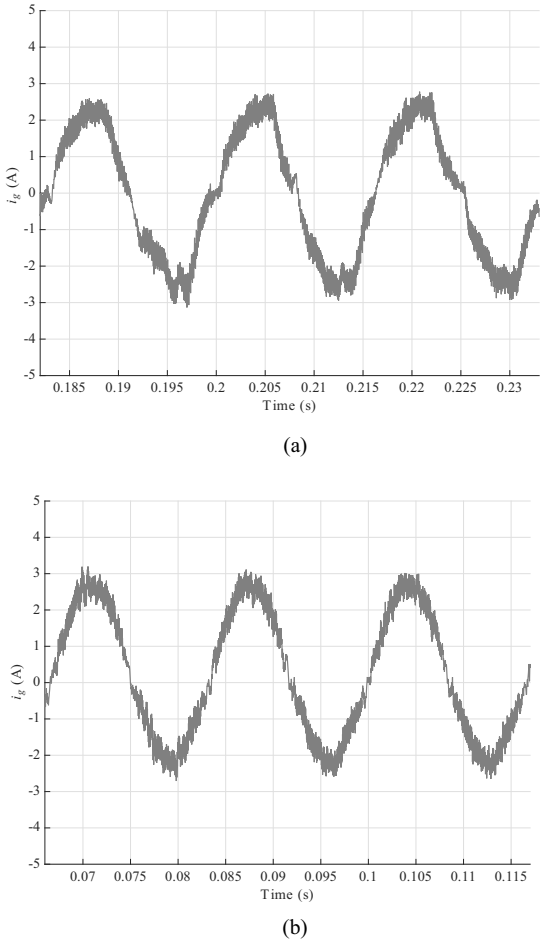


Figure 8: Grid current obtained for (a) the PI controller and (b) the hybrid controller.

version of the grid voltage, which is advanced in time to compensate the delays of the control loop, is used as the feedforward signal. Fig. 9(a) shows the evolution of the grid current for both feedforward signals. The current THD goes from 3.5% to 2.2%. Also the tracking error is improved as can be seen in Fig. 9(b) when the advanced version of the grid voltage is used.

C. Operation with compensation of dead-times

A dead-time $t_{DT} = 3\mu s$ is simulated for the turning on and off of the 3L-NPC transistors. A 10A current reference amplitude is set and the hybrid scheme is used without the volt-seconds compensation derived in (3). Fig. 10(a) shows the resulting grid current together with the reference. Near to the zero crossing some spikes can be observed which are similar to those shown in Fig. 4(b). Also a separation of the grid current from its reference occurs after each spike. This effect is minimized by using the compensation proposed in (3) and the resulting current is shown in Fig. 10(b). The current THD for the simulation with uncompensated dead-times is 7% and with the compensation goes down to 3%.

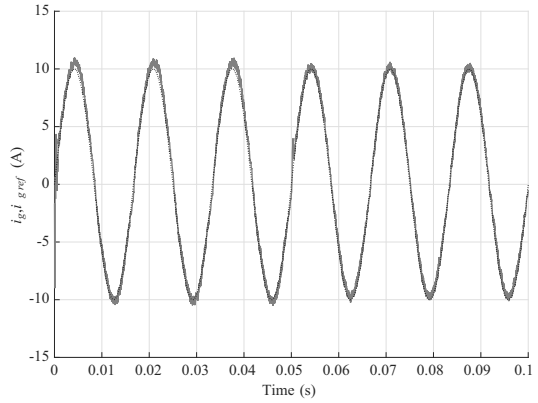
Table II: Percentage harmonic contents for the experimental grid voltage

Harmonic order	% of the fundamental
3^{rd}	7.78
5^{th}	1.88
7^{th}	0.23
9^{th}	0.63
11^{th}	0.03
13^{th}	0.12
15^{th}	0.16

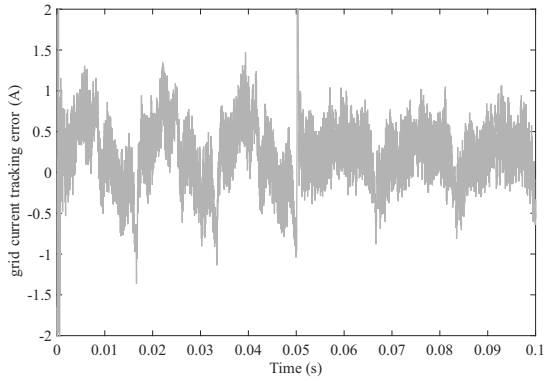
IV. Experimental tests

The validation of the previous techniques is made on an experimental test-rig developed by the authors [13], [14]. The grid voltage used in the experimental setup has a THD of 8% with the harmonics content shown in Table II.

The Fourier reconstruction of grid voltage $\hat{v}_g$ together with the measured voltage v_g is shown in Fig. 11, where $\hat{v}_g$ is running 2 sample periods ahead of v_g to compensate the delays of the control loop. A slight difference can be observed between v_g and $\hat{v}_g$ because the reconstruction is including just



(a)



(b)

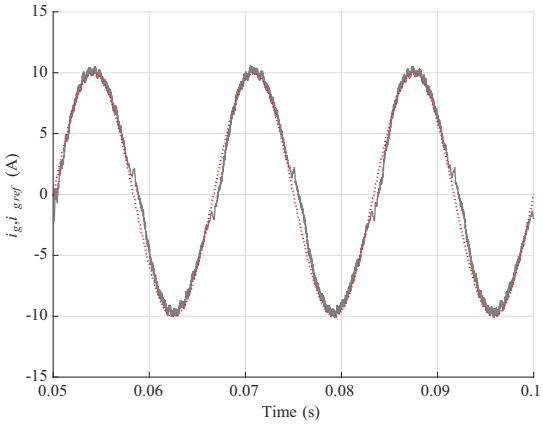
Figure 9: (a) Grid current evolution for different feedforward signals, (b) current tracking error.

the 3^{rd}, 5^{th}, 7^{th} and 9^{th} harmonics.

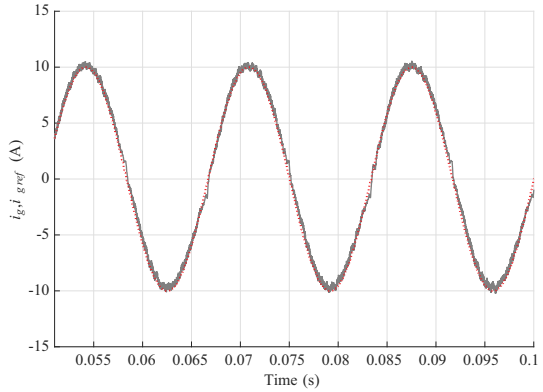
Figure 12 shows the evolution of the grid current for a 10A amplitude reference when the hybrid scheme is used. In this example the measured grid voltage v_g is used as the feedforward signal and there is no compensation of the dead-time resulting in the current spikes near to zero crossings. In this case, the resulting THD for the grid current is 5.3%. The resulting current when the dead-times compensation is applied is shown in Fig. 13. In this test the reconstructed grid voltage $\hat{v}_g$ is used as the feedforward signal. The spikes are successfully eliminated and the resulting THD is lowered to 3.9%. Fig. 14 shows the grid current and its reference for the same test.

V. Conclusion

A case study for designing the current control loop for grid connected inverters was presented. The design procedure is centered around three nonidealities such as a highly distorted grid voltage, the existence of dead-time effects and the delays introduced for the digital implementation of the control loop. The effects of this nonidealities are magnified because LCL filters with low inductance values are used to couple the inverter to the grid. A hybrid control scheme using a MPC



(a)



(b)

Figure 10: Grid current responses when (a) dead-times are simulated in the inverter and (b) when the volt-seconds compensation is applied.

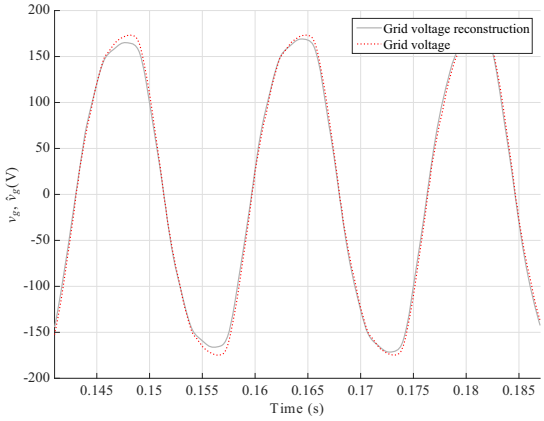


Figure 11: Measured grid voltage (v_g) and its reconstructed version ($\hat{v}_g$).

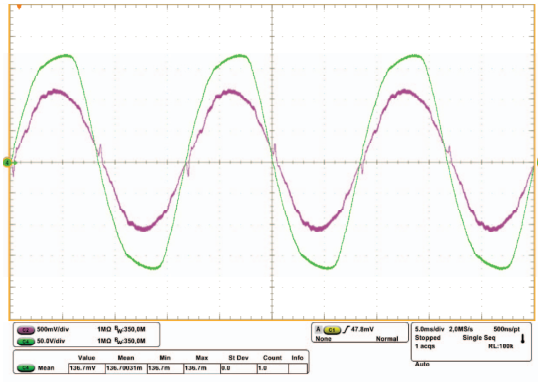


Figure 12: Experimental grid voltage and current without dead-times compensation when v_g is used as feedforward signal.

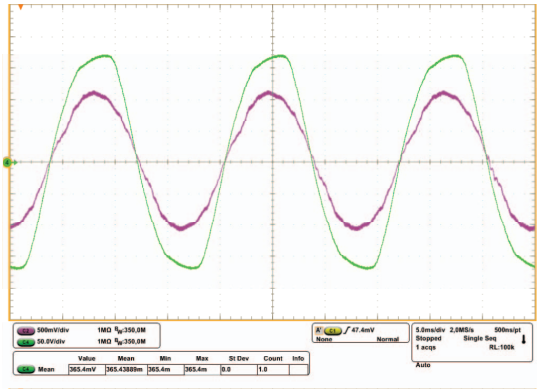


Figure 13: Experimental grid voltage and current with dead-times compensation when $\hat{v}_g$ is used as feedforward signal.

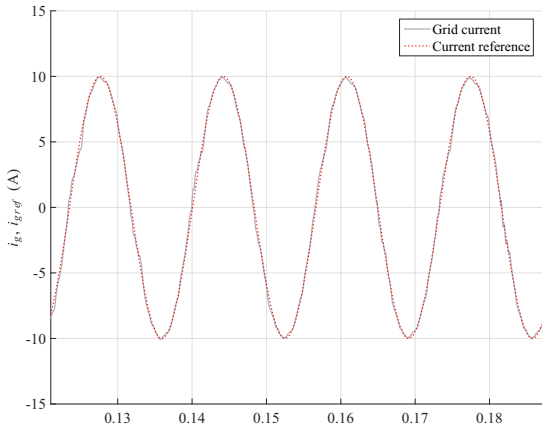


Figure 14: Experimental grid current (i_g) and its reference (i_{grf}).

and a proportional-integral action is proposed to improve the current tracking error when a distorted grid voltage is present. A decomposition in Fourier coefficients and a reconstruction of an ahead-of-time version for the grid voltage is proposed as a feedforward signal to overcome the problem of the delays in the control loop. Finally a compensation of the dead-time effects is implemented for the 3-level pulse width modulator. All these techniques combined are simulated and experimentally tested resulting in injected grid currents with THD even lower than that of the distorted grid voltage.

ACKNOWLEDGMENT

The authors would like to thank SENESCYT - Prometeo Project and Universidad Politecnica Salesiana in Ecuador for the financial support to this work.

REFERENCES

[1] "IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems," *IEEE Std 1547-2003*, pp. 1–28, July 2003.

[2] "Photovoltaic (PV) systems - Characteristics of the utility interface," *IEC 61727:2004*, pp. 1–23, December 2004.

[3] A. Reznik, M. Simoes, A. Al-Durra, and S. Muyeen, "Lcl filter design and performance analysis for grid-interconnected systems," *Industry Applications, IEEE Transactions on*, vol. 50, pp. 1225–1232, March 2014.

[4] R. Moreno, J. Pomilio, L. Pereira da Silva, and S. Pimentel, "Control of power electronic interface for renewable energy sources under distorted grid voltage," in *Clean Electrical Power, 2009 International Conference on*, pp. 407–414, June 2009.

[5] X. Wang, X. Ruan, S. Liu, and C. Tse, "Full feedforward of grid voltage for grid-connected inverter with lcl filter to suppress current distortion due to grid voltage harmonics," *Power Electronics, IEEE Transactions on*, vol. 25, pp. 3119–3127, Dec 2010.

[6] M. Liserre, R. Teodorescu, and F. Blaabjerg, "Multiple harmonics control for three-phase grid converter systems with the use of PI-RES current controller in a rotating frame," *IEEE Transactions on Power Electronics*, vol. 21, pp. 836–841, May 2006.

[7] Q.-N. Trinh and H.-H. Lee, "Improvement of current performance for grid connected converter under distorted grid condition," in *Renewable Power Generation (RPG 2011), IET Conference on*, pp. 1–6, Sept 2011.

[8] V. Yaramasu and B. Wu, "Model predictive decoupled active and reactive power control for high-power grid-connected four-level diode-clamped inverters," *Industrial Electronics, IEEE Transactions on*, vol. 61, pp. 3407–3416, July 2014.

[9] Y. Xingwu, J. Hongchao, and G. Wei, "Model predictive control of single phase grid-connected inverter," in *Power and Energy Engineering Conference (APPEEC), 2014 IEEE PES Asia-Pacific*, pp. 1–4, Dec 2014.

[10] X. Zhang, Y. Wang, C. Yu, L. Guo, and R. Cao, "Hysteresis model predictive control for high-power grid-connected inverters with output LCL filter," *Industrial Electronics, IEEE Transactions on*, vol. 63, pp. 246–256, Jan 2016.

[11] J. Viola, J. Restrepo, F. Quizhpi, and J. Aller, "Predictive control of a three-phase power converter coupled with LCL filter," in *Industrial Technology (ICIT), 2015 IEEE International Conference on*, pp. 2322–2326, March 2015.

[12] M. Reza, M. Ciobotaru, and V. Agelidis, "Accurate estimation of single-phase grid voltage parameters under distorted conditions," *Power Delivery, IEEE Transactions on*, vol. 29, pp. 1138–1146, June 2014.

[13] M. Gimenez, V. Guzman, J. A. Restrepo, J. Aller, A. Bueno, J. C. Viola, A. Millan, and A. Cabello, "PLATAFORMA: Development of an integrated dynamic test system to determine power electronics systems performance," *Revista de la Facultad de Ingenieria - UCV*, vol. 23, no. 3, pp. 91 – 102, 2008.

[14] J. Viola, J. Restrepo, F. Quizhpi, M. Gimenez, J. Aller, V. Guzman, and A. Bueno, "A flexible hardware platform for applications in power electronics research and education," in *Electrical Power Energy Conference (EPEC), 2014 IEEE*, pp. 1–6, Nov. 2014.