PLATFORM III: A NEW VERSION FOR THE INTEGRATED TEST SYSTEM FOR AC MACHINE DRIVES PERFORMANCE ANALYSIS

José Restrepo, María Isabel Giménez, Víctor Manuel Guzmán, José Manuel Aller, Alexander Bueno, Antonio Millán
Universidad Simón Bolívar, Grupo de Sistemas Industriales de Electrónica de Potencia
Apartado 89000, Caracas 1080-A, VENEZUELA
Telephone: 58-2-9063719, Fax: 58-2-9063712
E-mail: restrepo@usb.ve, mgimenez@usb.ve, vguzman@usb.ve, jaller@usb.ve

ABSTRACT.
This work presents the third version of the Integrated Test System "Plataforma", a test rig for experiments required to validate dynamically different types of new strategies and control schemes based on vector control theories, parametric estimation, and neural networks applied to AC machine drives; and to analyze the effect of these control strategies over the mains quality. The equipment includes the AC driver power stages, the mechanical load emulation stage, the instrumentation stage and the signal processing and control stage. Two main improvements have been performed: 1-An improved instrumentation stage. 2.- A dynamic load system implemented with a torque controlled DC motor. Due to its high versatility, this Test System can be used both in research laboratories and postgraduate courses.

1.- INTRODUCTION

Vector control theory [1] has allowed for the use of AC machine drives in many high dynamic performance applications previously reserved to DC machine drives. Nevertheless, a quick survey of the literature shows that most new control AC motor control schemes are tested under static load conditions, with very simple inertial loads. This is so because performing dynamic load tests on AC drives is very complex, requiring special equipment not usually available in the Laboratory. In response to this situation, the Industrial Systems and Power Electronics Group at the Simón Bolívar University has developed an Integrated Dynamic Test System (IDTS) for AC machine drives in order to validate the different types of new strategies and control schemes, mainly based on vector control principles in which the Group is interested [2,3,4].

The first Integrated Test System designed by the SIEP Group was assembled in 1998 and a first report was produced in 1999 [5]. The first version was mounted in an standard industrial enclosure, which was very compact and useful in hard environments, but it was difficult to reach all the measurement points. Therefore, a new design was produced [6], with a more modular layout and a better signal processing and control stage. This second version, was used to test the possibilities of the controlled rectifier using vector control techniques to correct the power factor, and to analyze induction machines and permanent magnet motors behavior under Field Oriented Method and Direct Torque Control techniques [7,9], among other applications.

To optimize Integrated Test System, it was required to get a better, noise-free acquisition system, to develop new tools in order to control the complete system, to incorporate a dynamic load emulator and to provide network connectivity, allowing direct loading of control algorithms developed in different work stations. The next sections present a detailed system description, with emphasis in the new developments introduced in this third version of the IDTS.

2.- HARDWARE DESCRIPTION

Figure 1 shows the IDTS block diagram. Heavy lines connect the blocks in the power stage, and fine lines connect the blocks in the instrumentation and control stages.

2.1.- The power stage

This stage includes three main active blocks: Rectifier (optional), Inverter (always present) and Chopper (optional), and two passive ones: the dc-link filter (always present) and the AC-line input filters (optional). Figure 2.A presents a frontal view of the IDTS, showing the inverter module (back, left), the chopper module (back, right) and the Data Acquisition and DSP boards (front, center). Figure 2.B presents the same test set-up pictured from the back; showing the three inverter (back, left) and the two Chopper IGBT modules (back, right) and the dc link filter (front, right)

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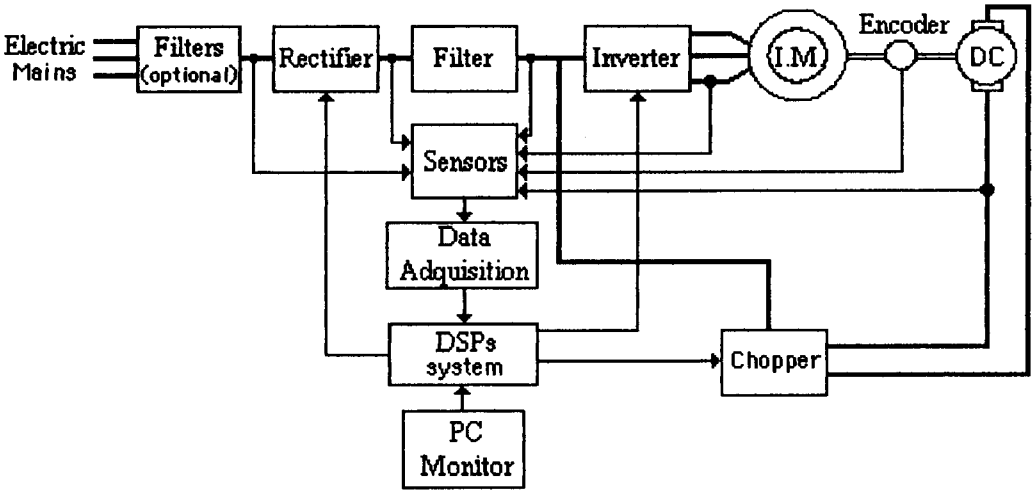
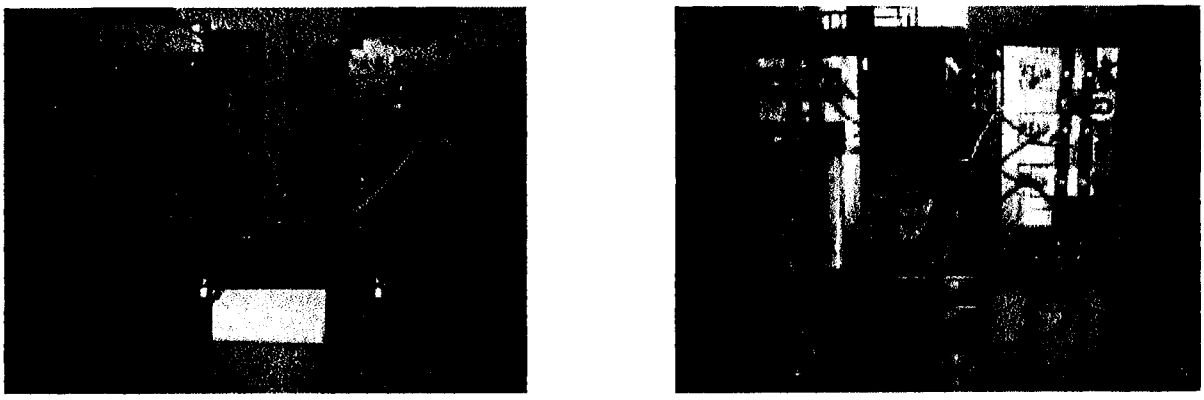


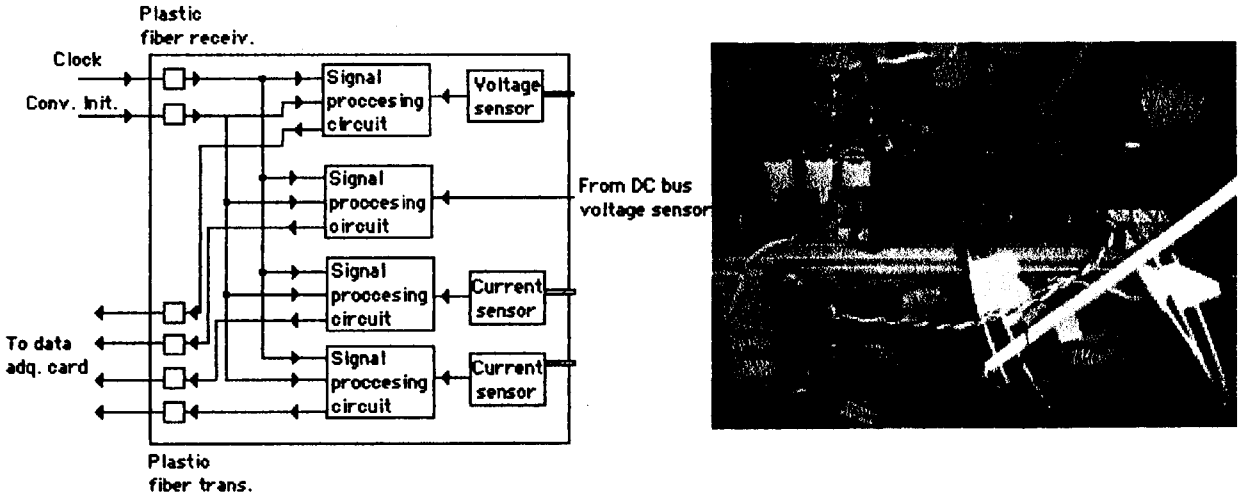
Fig. 1: Integrated Dynamic Test System Block Diagram



A: IDTS, front view

B: IDTS, back view

Figure 2. The Integrated Dynamic Test System.



A: Block diagram.

B: Circuit card photograph.

Figure 3. New Sensors Card

To ensure modularity a single converter circuit design was used in the three active power blocks. The Rectifier and Inverter blocks (identical and interchangeable) are implemented in a three-phase half-bridge configuration, with three dual IGBTs modules, type EUPEC FF50R12KF2, each one with and upper-lower device array and their corresponding antiparallel diode, rated at: Vce = 1200V, ic = 50A; ton= 0.4 μs toff = 0.2 μs and P = 400 W per IGBT. Each converter has an H31 heat sink and it is air cooled with a small fan. The thermal impedance is lower than 0.07 °C/W. The IGBT drive circuits have been implemented with three IHD280 integrate modules from CONCEPT. Protection circuits between each driver module and the IGBTs gate terminals have been included. Each driver consumes less than 2 W; the input voltage is 15 V and can deliver 200 mA. The turn-on and turn-off delay times are under 60 ns. A protection circuit is required to guarantee the driver circuit performance. Up to the third version, no snubber circuit has been incorporated, but it is possible to include different classical and loss-less snubber circuits to test the system performance with each configuration.
In the Chopper block a single-phase full-bridge configuration is used, which is actually an standard Rectifier/Inverter block with one dual IGBT module and its drive circuit omitted.

2.2.-The instrumentation stage

2.2.1.- Voltage and current measurements. New analog to digital conversion in the Sensors card.

As in the previous versions, the circuitry in the Sensors Card measures voltages and currents at the transformer primary and secondary terminals, currents at the inverter output, and the DC link voltage and current. Each card can hold two current sensors (LEM LA-55-P/SPI, Hall effect), one voltage sensor (LEM LV-25-P), and the circuitry for the DC bus voltage sensor (which is physically installed over the DC bus). The voltage sensors can work up to 500 Vrms at 8 kHz, with a ±0.05% precision, and a delay time less than 3 μs. The current sensors can measure up to 50 Arms at 150 kHz. These sensors isolate the Conversion circuit from the power circuits. Each Conversion circuit includes an amplification stage, two comparators to define the protection limits, and the analog to digital converter, whose output goes to the corresponding plastic fiber transmitter. The signal, once converted to digital form, is transmitted serially to the data acquisition and control card, via plastic fiber. For proper operation, the analog to digital converters require two signals, the clock and the conversion initialization, which come from the data acquisition and control card through two plastic fibers, whose receivers are located in the upper part of the sensors card. The modified sensors card block diagram is presented in Figure 3A. Figure 3B shows a photograph of one Sensors card. The two current sensors can be seeing at the card's upper right hand corner, the voltage sensor is at the upper left hand corner. The plastic fiber receivers and emitters can be seeing in the lower card's edge.

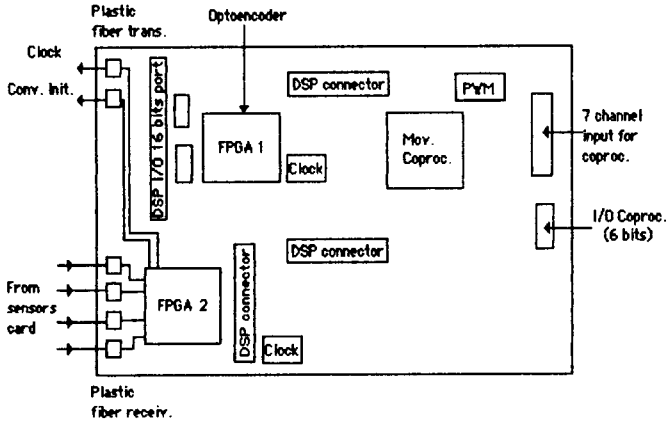
2.2.2.- Data acquisition system: The new Data Acquisition and Control card.

The new digital acquisition card incorporates the plastic fiber transmitters and receivers required for connection with the new Sensors cards. It also keeps the option based on the motion coprocessor (ADMC201) which makes it able to receive the already converted voltage and current signals, and pass them to the DSP, if the card is used with older Sensors cards. The motion coprocessor is connected to a PWM generator, a seven input channel connector and a six bits I/O port for the IGBT control signals. The card also holds two FPGA circuits. FPGA 1 is dedicated to speed measurements and it operates only when the encoder speed sensor is used, , while FPGA 2 processes the serial incoming signals from the A/D converters in the sensors cards, converting them from serial to parallel, in order to pass them to the DSP, and also controls the clock and the initialization signal that must be sent to the sensors cards, for the analog to digital converters. Three connectors located in the card's lower surface link this card with the DSP card.
Figure 4A shows the new data acquisition and control card block diagram; Figure 4B shows a photograph of one Data Acquisition and Control card (DAC card). The plastic fiber receivers and emitters can be seen in the left card's edge.

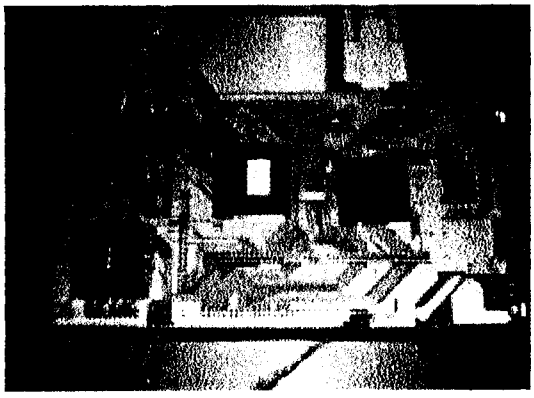
3.- DYNAMIC LOAD

As a last feature, a dynamic load system implemented with a torque controlled DC motor has been designed. The DC motor torque is controlled as a function of the shaft speed, in order to provide the AC motor with a shaft load that has the torque/speed characteristic of the mechanical load that is being emulated in the test. This new module will make possible to study the converter-motor dynamic system behavior using new control strategies under any type of load conditions,

included time changing loads. The basic routines for controlling the DC motor torque have been programmed, as shown in Figure 5. This work is in progress, dynamic test results obtained will be presented in another work.



A. Block diagram.



B. Circuit card photograph.

Figure 4. New DAC card.

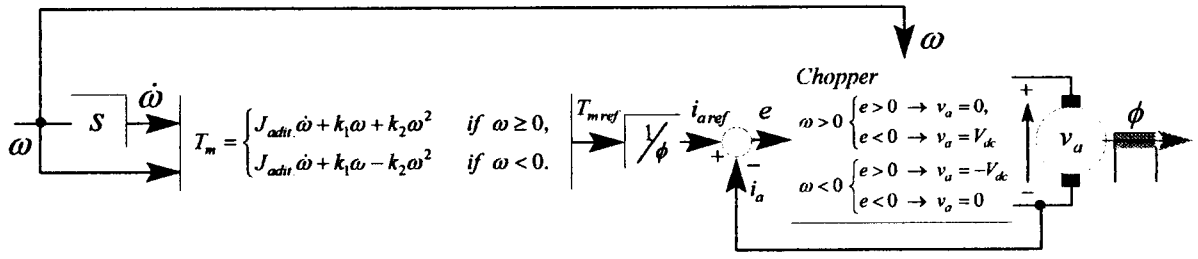


Figure 5.- Control strategy for the dynamic load

4.- RESULTS

In order to test the new sensor card and data acquisition and control card, a delta control technique was programmed in the DSP, and current measurements were performed with the second version motion coprocessor system and with the new circuitry. Figure 6 presents two AC induction motor phase currents, directly measured with a 500 MHz digital oscilloscope (Tek. TDS3054, 2GS/s) using a Hall effect current probe. The commutation band defined by the delta modulation can be clearly observed in this figure.

Figure 7 shows the currents sensed with the Hall effect sensors, just before the A/D converters as measured in the old (Figure 7A) and the new Sensors card (Figure 7B). As can be observed, both signals present the phase current switching between the prefixed limits, but the commutation band for the current in the old circuit is broader than in the new version due to noise effects, because the first signal had to travel from the sensor card to the data acquisition card, while in the second case, the A/D converter is right behind the sensor output.

Figure 8 presents the phase currents acquired by the DSP systems for the two versions (Figure 8A, old system, Figure 8B, new system). The waveforms for the third version are closer to the actual current waveforms presented in Figure 6. This accuracy is a crucial point for a Test System, when a new strategy must be validated. The acquisition with the second version looks "cleaner", which means that it has lost part of the phase current information (the commutation band), giving less reliable results than those obtained with the third version.

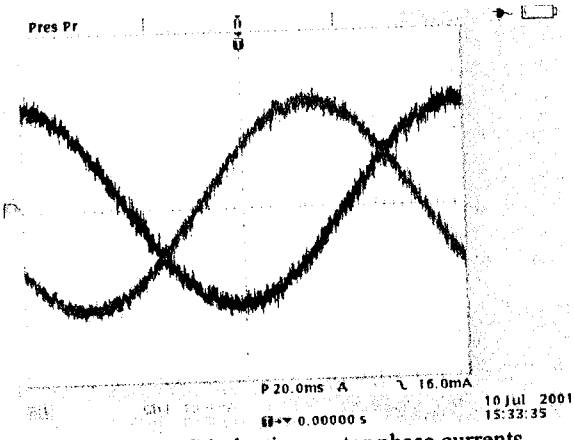
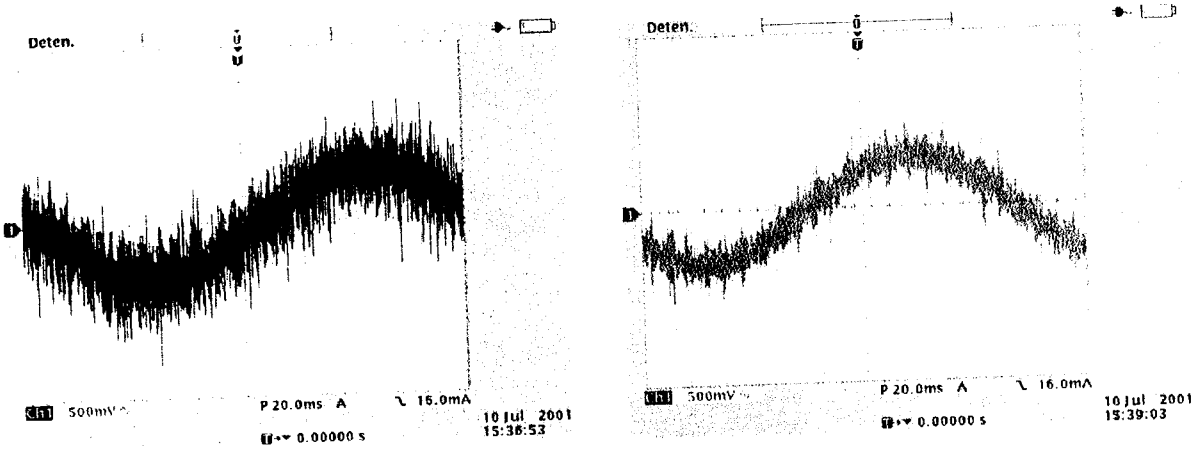


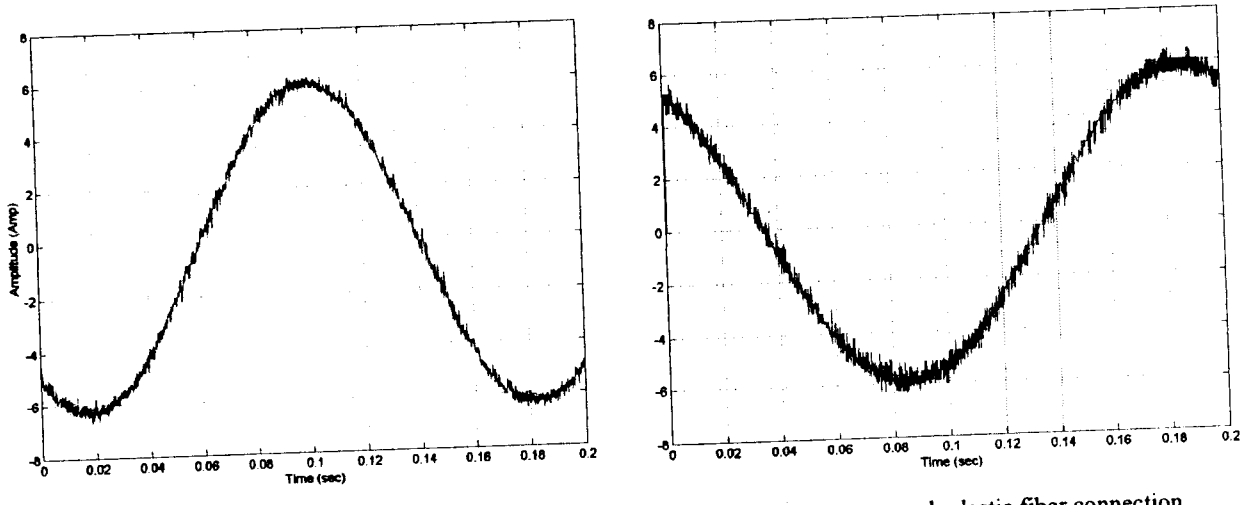
Figure 6.- AC induction motor phase currents.



A: Old Sensors card, wire connection.

B: New Sensors card, plastic fiber connection.

Figure 7.- Sensed phase current at the A/D input.



A: Old Sensors card, wire connection.

B: New Sensors card, plastic fiber connection.

Figure 8.- Phase current acquired by the second version DSP system.

7.- CONCLUSIONS

The Plataforma III Test System developed is able to perform many different control strategies including spatial vector control, neural network control, DTC control, PWM modulation, delta-modulation, mains harmonic reduction, on line parametric estimation, and sensorless speed measurement. Changing the control strategy in the Test System just implies writing a new subroutine for the DSP. Usually no major changes in the hardware layout will be necessary. The new features included in the third version offer a more reliable system. The versatility, reliability and precision of the Test System make a very convenient resource for researchers and post-graduate students, specially with the new designed tools to facilitate the programming work.

8.- REFERENCES

1. W. LEONHARD. *Control of Electrical Drives, Springer-Verlag*, Berlin, Heideberg, 1985.
2. A. BUENO, J.M. ALLER. *Adaptive Control of Induction Machine by Oriented Field using Neural Networks.* International Conference on Electrical Machines. ICEM'96. Vol. II, pp. 223-228. Vigo, Spain. September 1996.
3. J. RESTREPO, T. PEREZ, M. I. GIMENEZ. and V. GUZMAN. *DSP Implementation of AC-Machine Sensorless Speed Measurement System Using the Wigner Distribution. 7th European Power Electronics and Applications. EPE'97.* Vol.4, pp. 524-527, September 1997, Trondheim, Norway.
4. J. J. REIMONDEZ, M. I. GIMENEZ, V. M. GUZMAN, R. MONCADA, J. A. RESTREPO, *Speed and Position Control of Brushless DC Machine employing Neural Networks.* 7th European Conference on Power Electronics and Applications, EPE'97. Vol. 2, pp. 465-470, Trondheim, Norway, September 1997.
5. M. I. GIMÉNEZ, J. M. ALLER, F. QUINTLRO, V. M. GUZMÁN, J, A. RESTREPO, *An Integrated Test System for AC Machine Drives Performance Analysis.* Proceedings of the 8th European Conference on Power Electronic and Applications EPE'99, CD, Sep. 1999
6. M. I. GIMÉNEZ, J. A. RESTREPO, V. M. GUZMÁN, J. M. ALLER, A. BUENO, *Plataforma II: Un sistema integrado de pruebas para el análisis del rendimiento de las estrategias de control de motores,* Seminario Anual de Automática, Electrónica Industrial e Instrumentación SAAEI-2000, pp. 259-262, Sept. 2000.
7. T. PAGA, A. BUENO, M. I. GIMÉNEZ, J. A. RESTREPO, V. M GUZMÁN, J. M. ALLER, *Sensorless Speed Control of the Induction Machine Combining Field Oriented Method and DTC,* Proceedings of the Third IEEE International Caracas Conference on Devices, Circuits and Systems, ICCDCS-2000, Cancun, Mexico, pag. P79-1 a P79-6, Marzo 2000.
8. J. A. RESTREPO, J. M. ALLER, T. PAGÁ, A. BUENO, M. I. GIMÉNEZ, V. M. GUZMÁN, *Direct Torque Control of the induction machine using field oriented method and time frequency transformation for speed estimation and parameter adaptation,* Proceedings of the International Conference on Electrical Machines ICEM 2000, Pp 1105-1109, Aug 2000.

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