Two-Phase Active Power Filter Direct Current Control with Capacitor Voltages Estimation and Balance

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***Abstract*—In this paper an active power filter is presented based on a multilevel converter. The active power filter is intended to be used in domestic applications where reactive power compensation in two-phase networks is required. An innovative technique to balance the DC bus voltages of the power converter capacitors is proposed and also an estimation algorithm for those voltages is developed, allowing for an operation of the power filter with reduced sensors number.**

***Index Terms*—active power filter, multilevel converter, reactive power, estimation method.**

I. Introduction

The increasing number of nonlinear loads used nowadays in domestic electric installations and the projections made for future years led to the necessity of countermeasures to cope with the negative effects of current harmonics. Active power filters (APF) have been traditionally designed and produced to operate in industrial applications, nonetheless the lower costs of power electronics switches and microprocessors have made possible to include them in the compensation of reactive power in domestic applications [1]. While the use of single-phase and three-phase topologies for APF is widely reported in the technical literature [2],[3],[4],[5],[6],[7], there is a lack of papers addressing two-phase applications. This type of electric installations is very common in those countries having 110Vrms as the standard voltage in home wiring where typically a second phase must be added to obtain 220Vrms in those outlets dedicated to heavy loads (electric dryers, electric cooktops, etc.) The work presented in [8] is one of the few addressing the problem of reactive power compensations in two-phase installations, where the use of an H-bridge 4-switch voltage source converter (VSC) is proposed to compensate the current harmonics introduced by a two-phase spot welder. In [9] the authors have proposed the use of a multilevel VSC operating as a two-phase shunt APF. By using the cascaded H-bridge topology, shown in Fig. 1, it is possible to obtain 5-level switched voltages with less harmonic content allowing for a size reduction of the inductor used to couple the converter to the grid. This topology has as a drawback that a balancing of the capacitor voltages is required to assure stable values for the VSC voltage space vectors. Also the used multilevel topology requires more voltage sensors to operate. In the present work these issues are addressed by proposing a balancing method for the DC voltages in the bus of each H-bridge. Additionally an estimation method for each capacitor voltage is developed based on the method proposed in [10] where measuring of input/output VSC currents and knowing of switching state of the converter are used to obtain an estimated value of each voltage. The operation of the APF is tested by simulations when a direct current control is implemented [9],[11].

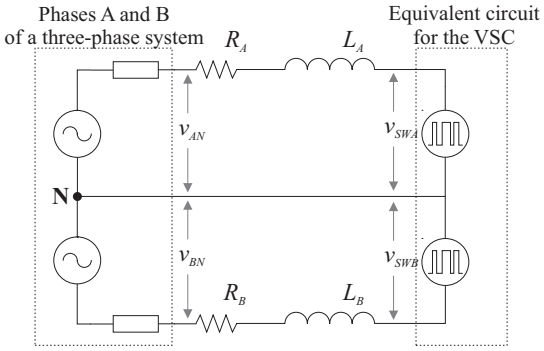


Figure 2: Equivalent circuit for the two-phase active power filter.

II. Current loop control

Figure 2 shows the equivalent circuit for the APF connected to the grid. The VSC is controlled by a direct current control (DCC) algorithm which is based in the minimization of a quadratic current error function as is reported in [9]. The method uses the discrete predictive expression (1) for the VSC current expressed as a function of the switching voltage (V_{SW}), the grid voltage (V_{AN}), the inductance value (L_A) and

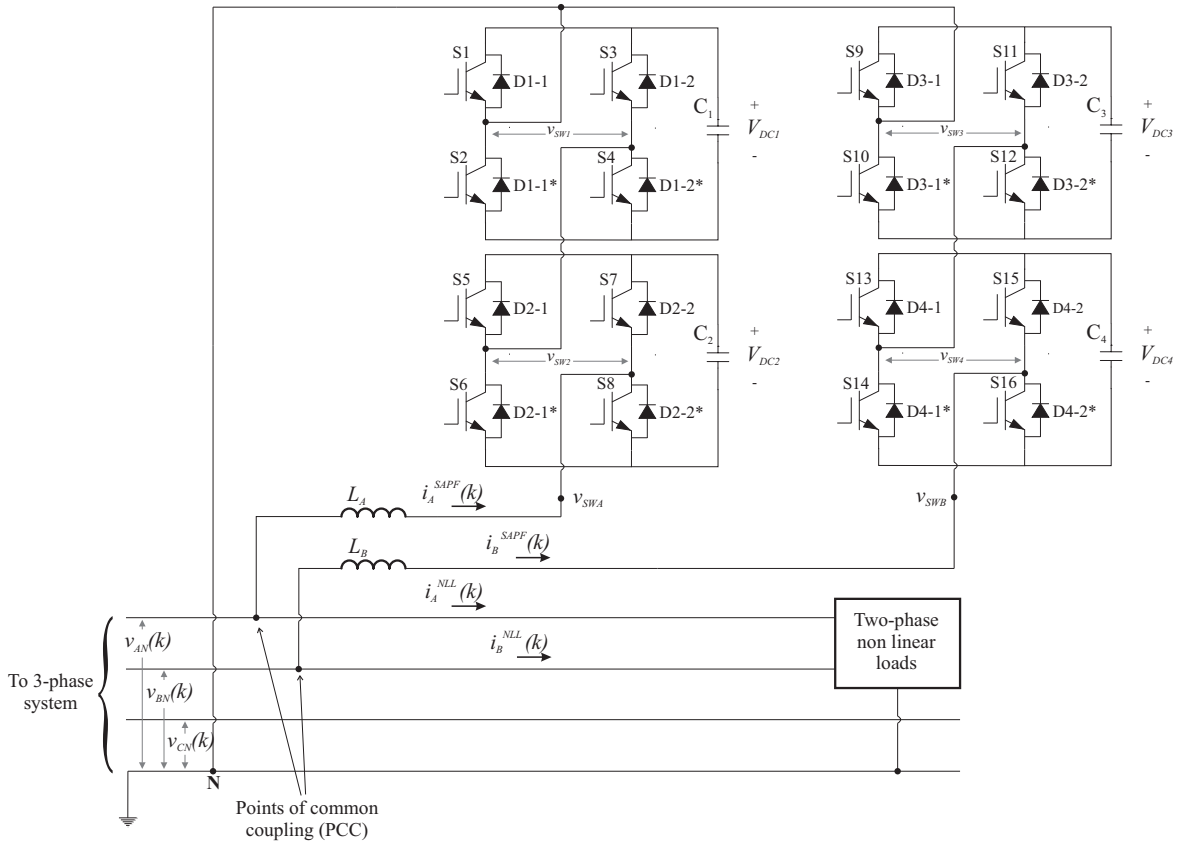


Figure 1: Schematic circuit for the two-phase active power filter.

the intrinsic resistance (R_A) associated to the inductor.

$$i_A^{APF}(k+1) = i_A^{APF}(k) + \frac{Ts}{L_A}(V_{AN}(k) - R_A\, i_A^{APF}(k) - V_{SW}(k)) \quad (1)$$

where Ts is the sampling period. The quadratic expression computes the difference between the current reference and the predicted current in the instant (k+1), resulting in

$$\varepsilon = (i_{A\,ref}^{APF}(k) - i_A^{APF}(k+1))^2 \quad (2)$$

The multilevel VSC has 5 voltage levels in each phase going from $+2V_{DC}$ to $-2V_{DC}$ in steps of V_{DC}. In Table I the voltage levels and the corresponding switching states are shown, where on and off states for each switch are represented by "1" and "0" respectively. As can be noted voltage levels $+V_{DC}$, 0 and $-V_{DC}$ can be obtained with more than one switching state. This redundancy will be used for the balancing method proposed in the next section. For each control period the DCC algorithm computes the quadratic error (2) between the current reference and the predicted current, determining which of the 5 voltage levels gives the smaller current error. The obtained value is selected to be applied in the next control cycle. A block diagram for the involved variables is shown in Fig. 3, where are also included the blocks corresponding to the voltage balancing and the voltage estimation methods which are explained in next two sections.

Table I: Voltage levels, switching states and changes in capacitors charge for one phase of the APF

Voltage levels	Switching states								Change in capacitors charge	
	S1	S2	S3	S4	S5	S6	S7	S8	C_1	C_2
$+2V_{DC}$	1	0	0	1	1	0	0	1	+	+
$+V_{DC}$	1	0	0	1	1	0	1	0	+	0
	1	0	0	1	0	1	0	1	+	0
	1	0	1	0	1	0	0	1	0	+
	0	1	0	1	1	0	0	1	0	+
0	1	0	1	0	1	0	1	0	0	0
	1	0	1	0	0	1	0	1	0	0
	0	1	0	1	1	0	1	0	0	0
	0	1	0	1	0	1	0	1	0	0
	0	1	1	0	1	0	0	1	-	+
	1	0	0	1	0	1	1	0	+	-
$-V_{DC}$	0	1	1	0	1	0	1	0	-	0
	0	1	1	0	0	1	0	1	-	0
	1	0	1	0	0	1	1	0	0	-
	0	1	0	1	0	1	1	0	0	-
$-2V_{DC}$	0	1	1	0	0	1	1	0	-	-

III. VOLTAGE BALANCING METHOD

When a VSC is operated as an active power filter the voltage of the DC bus capacitors must be controlled to assure stable and safe operation of the whole system. A voltage reference is typically set for each DC bus and a proportional-integral

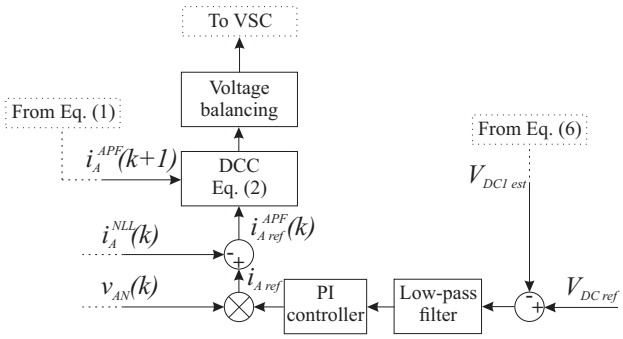


Figure 3: Blocks diagram for the involved variables.

(PI) controller is in charge of generate the current reference by multiplying its output with the acquired grid voltage signal as can be seen in Fig. 3. The current reference can be obtained also by others method based on a phase lock loop (PLL) or calculation of instantaneous power. The used method, however, does not affect the behavior of the current loop. A low pass filter is added at the input of the PI controller so that any component of 2nd harmonic (100 or 120Hz) is rejected and its effect does not propagate in the control loop. To implement the voltage balancing method the redundant switching states of the multilevel VSC are used. The last two columns of Table I show the change in the electric charge of capacitors C_1 and C_2 for each switching state when current i_A^{APF} has the direction indicated in Fig. 1. The sign " $+$ " represents an increase of capacitor charge and therefore of its voltage, sign " $-$ " represents a decrease of charge and "N" means no change occurs for that switching state. If current i_A^{APF} has the opposite direction, the table is modified interchanging signs " $+$ " and " $-$ ". The DCC algorithm explained in the previous section chooses the more appropriate voltage level so that the current error is minimized. If the selected voltage level has redundant switching states (i.e. levels $+V_{DC}$, 0 and $-V_{DC}$) the voltage balancing method can choose the best switching state among the available for the selected voltage level, so that any unbalance in the voltages of capacitors C_1 and C_2 can be corrected. In every control cycle the most charged capacitor is discharged if a " $-$ " switching state is available or the less charged capacitor is charged if there is a " $+$ " state for the selected voltage level. This procedure applied continuously achieves a balance for the voltages of both capacitors as it will be shown in the simulation section.

IV. Voltage estimation method

The measuring of currents i_A^{APF} and i_B^{APF} entering or leaving both phases of the VSC is required to implement the current loop. This measuring can be used to estimate the voltages in each capacitor of the VSC, reducing in this manner the number of required sensors. The magnitude of current flowing through a particular capacitor is the same of the current flowing for the corresponding VSC phase. The sign of that current, however, depends on the switching state being activated by the control algorithm. This can be expressed as

$$i_{C_j} = i_A^{APF}\, SS_j \tag{3}$$

where SS_j is the switching state of the H-bridge where the capacitor is attached to. The Table II gives the possible values for SS_j.

Table II: Switching states for each H-bridge and the corresponding V_{SW} voltages

SS	V_{SW}
"+1"	$+V_{DC}$
"−1"	$-V_{DC}$
"0^u"	0
"0^d"	0

In continuous time the voltage in each capacitor can be written as

$$V_{DCj\,est} = \frac{1}{C_j}\int_0^t i_{C_j} dt + V_{DCj}(0) \tag{4}$$

If a sampling time T_s is used and it is supposed that current i_{C_j} does not vary during this time, the previous expression can be written in discrete time as

$$V_{DCj\,est}(k) = \frac{T_s}{C_j} i_{C_j}(k) + V_{DCj}(k-1) \tag{5}$$

and using (3)

$$V_{DCj\,est}(k) = \frac{T_s}{C_j} i_A^{APF}(k)\, SS_j(k) + V_{DCj}(k-1) \tag{6}$$

V. Simulations

The operation of the whole system was performed by using MATLAB/Simulink. In Fig. 4 the block diagram of the simulated system is shown, where 2 highly nonlinear loads composed by half wave diode rectifiers are connected to the grid. The APF is connected in parallel to the nonlinear loads by means of 2 coupling inductors with 10mH inductance value and an intrinsic resistance value of 10mΩ. Voltage reference for each DC bus was set to 170V, PI controller proportional gain was set to $k_p = 0.4e-3$ and integral gain was $k_i = 0.5e-3$, while low-pass filter cut frequency was set to 20Hz. Capacitors in the DC links were set to 2200μF and the sample time for the system was 100μs.

A. Operation of the system with the active filter disabled

The current in phase "a", for the system operating with the the APF disabled, is shown in Fig. 5a. The harmonic content in this case is shown in Fig. 5b with a resulting THD of 43.85%, which is similar to the one obtained for phase "b" [9].

B. System with full DC voltage measurements and algorithm for voltage balancing

The objective of the controller is to compensate the current taken or injected from the grid, seen from the PCC. The current to/from the grid becomes sinusoidal, and in this work, in phase

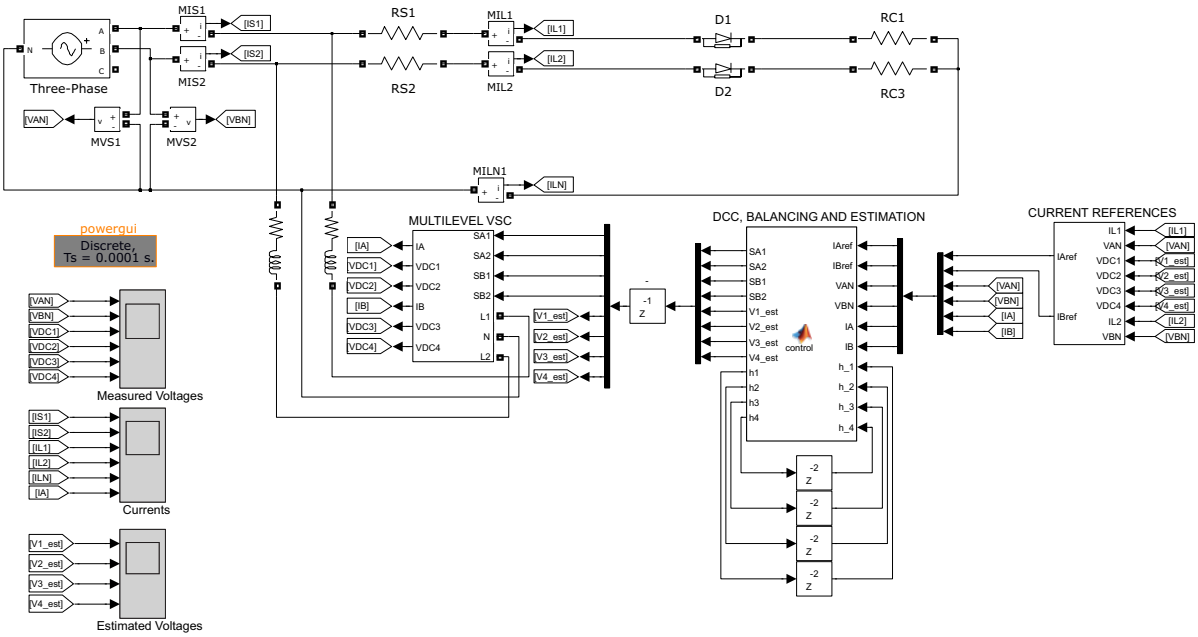
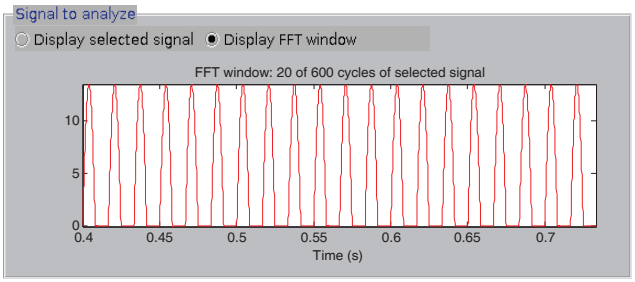
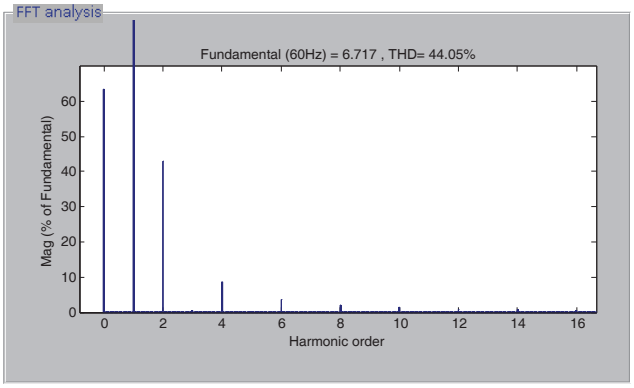


Figure 4: Blocks diagram for the simulated system.

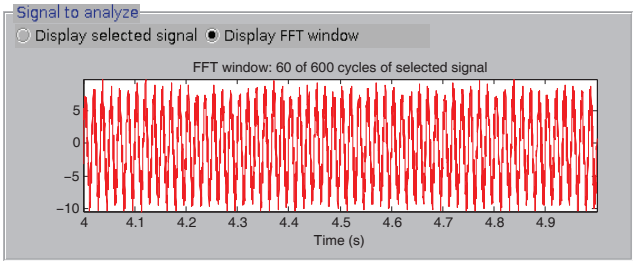


(a) Phase a current

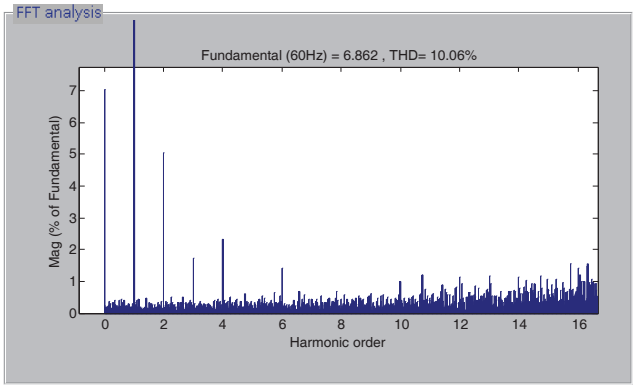


(b) Phase a harmonic content

Figure 5: Phase a current for the APF disabled



(a) Phase a current



(b) Phase a harmonic content

Figure 6: Phase a current for the APF enabled

with the grid voltage. However, this can be easily changed to provide or take reactive power from the grid.

Figure 6a shows the resulting current for phase "a", and Fig. 6b shows the harmonic content of the same current. The resulting THD is reduced from 43.85%, when the APF is disabled, to 11.22% when the APF is enabled and all the DC link voltages are measured. This shows the improvement in the harmonic content due to the operation of the APF.

Besides the improvement in the power quality, with the compensation of the harmonics to/from the grid, the voltage in the capacitors associated to each cell need to be balanced. This requires measuring or estimating the voltage in each DC link capacitor, and applying the proper switching pattern to balance

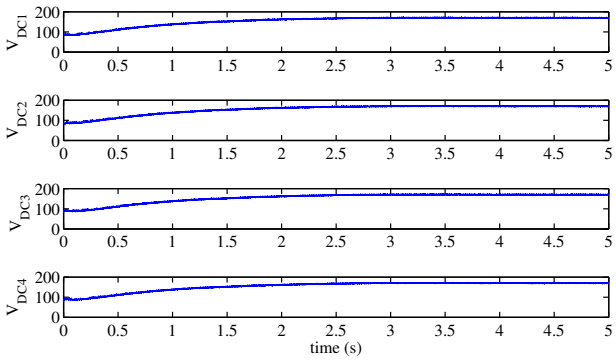


Figure 7: Evolution of measured capacitors voltages.

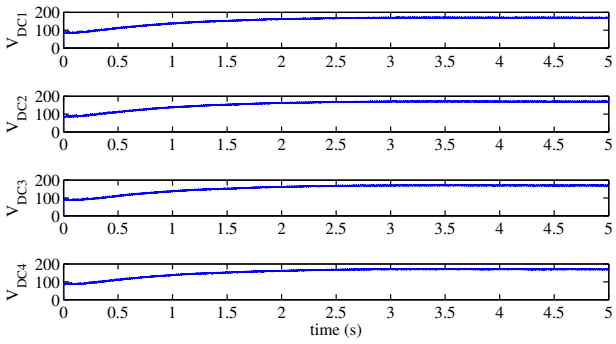


Figure 8: Evolution of estimated capacitors voltages.

the voltage in the capacitors. Figure 7 shows the evolution of the voltage in capacitors C_1 and C_2 , in phase A, and C_3 and C_4 in phase B. They have a similar evolution along the time, reaching a stable value of approximately 170 V which is set by a voltage reference as mentioned before in Fig. 3. In this way the voltage is shared equally between each cell, and the stress in the power devices is equalized.

C. System with estimated DC voltage and algorithm for voltage balancing

An additional objective of the control system is to estimate the DC bus voltage in each cell, in this way the number of voltage sensor can be reduced. Figure 8 shows the estimated voltages in all capacitors where, again, all voltage reach the reference of 170 V. Figure 9 shows the error between estimated and measured voltages in capacitor C_1 where the accuracy of the estimation can be appreciated.

The current taken from the grid while the active filter is enabled, using the estimated DC link voltages has a THD, of 14.83%. This result is comparable with the one obtained using the measured DC link voltages. The comparison of the system for different operating conditions is done first for the case with the active filter disabled, second the active filter is enabled with a completed measurement of the DC link voltages and third the active filter is enabled but the DC link voltages are estimated. For the cases with the active filter enabled, the controller uses

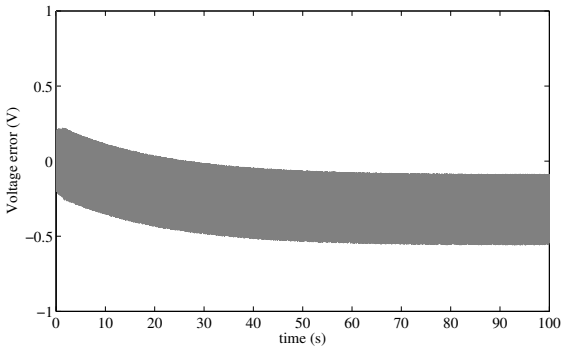


Figure 9: Error between measured and estimated voltages.

Table III: Results of the system's simulation for a) APF disabled, b) APF enabled with full DC link voltage measurement and c) APF enabled with estimated DC link voltages.

Phase	THD filter disabled	THD for APF enabled with voltage balancing and full measurement	THD for APF enabled with voltage balancing and estimated DC link voltages
a	43.85%	11.22%	14.83%
b	43.85%	10.22%	14.22%

an algorithm for balancing the DC link voltages through the proper selection of the switching pattern in the converter. Also, the system uses a PI controller to provide the reference for the current loop. The values for the different tests are presented in Table III.

This table shows that the operation of the controller improves the harmonic content of the current taken from the grid, with THDs of 11.22% and 14.83% for the fully measured DC link voltages and with the estimated values respectively. The fully sensed case provides better results, but the savings in sensors makes the estimated case a good alternative, with a relatively low impact on the resulting THD.

VI. Conclusion

This work has proposed a controller for an active filter, with the capability of balancing the DC link voltage in all the cells of a given branch of a multilevel converter. This provides a better power sharing among the cells in the multilevel converter. The proposed system also includes a PI controller for the total DC link voltage, acting on the reference of the current loop, regulating in this way the active power taken by the active filter. From the results it is clear that the system is able to compensate the harmonic content of the current taken from the grid, by reducing the THD, for highly non linear loads. Also, the estimation of the DC link voltages provides a good tradeoff between the quality of the compensation and the cost of implementing the active filter. The impact on the THD due to the use of estimated DC link voltages is low, with a difference on THDs of about 3%. Future works will include experimental validation on the multilevel platform reported in [12].

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REFERENCES

[1] B. Exposto, H. Goncalves, J. Pinto, J. Afonso, and C. Couto, "Three phase four wire shunt active power filter from theory to industrial facility tests," in *Electrical Power Quality and Utilisation (EPQU), 2011 11th International Conference on*, pp. 1–5, Oct 2011.

[2] M. El-Habrouk, M. Darwish, and P. Mehta, "Active power filters: a review," *Electric Power Applications, IEE Proceedings -*, vol. 147, pp. 403–413, Sep 2000.

[3] B. Singh, K. Al-Haddad, and A. Chandra, "A review of active filters for power quality improvement," *Industrial Electronics, IEEE Transactions on*, vol. 46, pp. 960–971, Oct 1999.

[4] J. Restrepo, J. Viola, J. Aller, and A. Bueno, "Algorithm evaluation for the optimal selection of the space vector voltage using dpc in power systems," in *Power Electronics and Applications, 2007 European Conference on*, pp. 1–9, Sept 2007.

[5] S. Leng, W. Liu, I.-Y. Chung, and D. Cartes, "Active power filter for three-phase current harmonic cancellation and reactive power compensation," in *American Control Conference, 2009. ACC '09.*, pp. 2140–2147, June 2009.

[6] J. Viola, J. Restrepo, J. Aller, J. Aller, R. Harley, and T. Habetler, "Simplified Control Structure for Current Control of Single Phase Rectifiers Using COT-ANN-PWM," in *International Joint Conference on Neural Networks, 2007. IJCNN 2007*, pp. 1370–1374, Aug. 2007.

[7] B. Crowhurst, E. El-Saadany, L. El Chaar, and L. Lamont, "Single-phase grid-tie inverter control using dq transform for active and reactive load power compensation," in *Power and Energy (PECon), 2010 IEEE International Conference on*, pp. 489–494, Nov 2010.

[8] H. Hojabri and H. Mokhtari, "A new power quality enhancement method for two-phase loads," in *Power Electronics, Drives and Energy Systems, 2006. PEDES '06. International Conference on*, pp. 1–5, Dec 2006.

[9] H. Bueno, M. Fajardo, F. Quizhpi, J. Viola, and J. Restrepo, "Shunt active power filter for harmonic compensation of two-phase nonlinear loads," in *2014 IEEE PES Transmission & Distribution Conference and Exposition (T&D)*, (Medellin), pp. 1–6, IEEE, Sept. 2014.

[10] J. Viola, E. Baethge, A. Berzoy, J. Restrepo, and F. Quizhpi, "DC voltage estimation methods for multilevel converter operating with reduced number of sensors," in *2014 IEEE 5th Latin American Symposium on Circuits and Systems (LASCAS)*, pp. 1–4, Feb. 2014.

[11] A. Berzoy, J. Viola, and J. Restrepo, "Voltage space vector's computation for current control in three phase converters," *Revista Facultad de Ingenieria*, vol. 0, pp. 45–56, Mar. 2012.

[12] J. Viola, J. Restrepo, F. Quizhpi, M. Gimenez, J. Aller, V. Guzman, and A. Bueno, "A flexible hardware platform for applications in power electronics research and education," in *Electrical Power Energy Conference (EPEC), 2014 IEEE*, pp. 1–6, Nov. 2014.