Abstract—This work presents a dual converter employed as a rectifier with power factor regulation and bidirectional power flow. The active and reactive power flowing into the converter is controlled using an optimized direct power control algorithm. The multilevel structure of the converter is exploited to control the voltage level in each sub converter by selecting the modulation method from one commonly found in the literature, with the option of clamping one of the sub converters. These modulation methods are used to control the power taken by each sub converter, providing limited DC link voltage regulation. The system is first simulated in SIMULINK and the results were experimentally validated using a digital signal processor (DSP) based test rig.

I. INTRODUCTION

Nowadays, multilevel inverters continue to be a topic of intense research [1]–[4], and several modulation techniques have been reported with numerous advantages over conventional two-level inverters [5]–[8]. One important advantage is the possibility to improve harmonic content for the synthesized voltage, with a reduced number of commutations [5]. Another advantage of multilevel converters is the possibility to reach higher voltage levels and higher power rating with power devices having lower breakdown voltages [5], [9]. The increase in components in multilevel converters results in a corresponding increase in the number of valid commutation states, and this in smoother changes in the state variables of the system and its ensuing reduction in the output voltage \( \frac{dv}{dt} \).

Among many existing multilevel topologies, the dual converter structure has the advantage that multilevel operation can be obtained by using two standard two-level converters. Since it was proposed [10], this topology has been used mainly for control of induction motors with open-end stator windings [3], [4], [11]. Others applications for this topology are found in photovoltaic generation systems [12], [13]. Multilevel topologies have been used also as VAR compensators [14], but there are no reported applications of the dual converter working as an active front end (AFE) rectifier with controlled power factor. The possibility of its use as an active filter was suggested in [12], however.

In this work, a synchronous rectifier is obtained by connecting the center tap of each sub converter’s leg to the open end of a three-phase transformer secondary windings. The converter’s block diagram is shown in Fig. 1(a) where the direct power control (DPC) algorithm proposed in [15] is used to control the dual converter. In this version of the DPC algorithm, the optimum voltage space vector to be synthesized by the dual converter, in each control cycle, is obtained in a straight forward manner by using a closed form formula, derived directly from the expressions of the instantaneous active and reactive power at the converter’s input. Additionally, since the dual converter’s structure has two independent DC links, it was shown that different modulation methods can be used to control the power flow into each DC link.

The principle of alternate-sub-hexagonal center PWM switching strategy proposed in [3] for standard SVM-PWM is extended to the generalized space vector PWM method in this paper.

The paper is organized as follows: section II shows a description of the dual converter’s space vector computation derived from the active and reactive power demands. Section III presents the general PWM strategy used to obtain the rectifier’s voltage vector. Section IV shows a generalization of the principle of alternate sub-hexagonal center initially proposed in [16]. Finally in section V, the proposed scheme is analyzed by simulations and by an experimental test.

II. SPACE VECTOR COMPUTATION

The control algorithm used in this work relies in the computation of the dual converter space vector \( \vec{v}_r \) required by the active and reactive power demands. From Fig. 1(b) the system can be modeled with the following first order differential equation.

\[
\begin{align*}
\vec{v}_s(t) &= R_{AF} \vec{\dot{i}}_s(t) + L_{AF} \frac{d\vec{i}_s(t)}{dt} + \vec{v}_i(t) \\
\end{align*}
\]

A discrete version of the system model can be obtained by using a first order approximation of (1).

\[
\begin{align*}
\vec{v}_s(k) &= R_{AF} \vec{\Delta i}_s(k) + L_{AF} \frac{\vec{i}_s(k + 1) - \vec{i}_s(k)}{T_s} + \vec{v}_i(k) \\
\end{align*}
\]

where \( T_s \) is the sampling time.

The instantaneous active and reactive power in the system can be computed using the system’s state variables described
in \((x, y)\) coordinates as follows,

\[
P = v_{ux}i_{ux} + v_{uy}i_{uy} \\
q = v_{uy}i_{ux} - v_{ux}i_{uy}
\]  

For a required instantaneous active and reactive power, the system current can be obtained as

\[
i_{ux} = \frac{p \cdot v_{ux} + q \cdot v_{uy}}{v_{xx}^2 + v_{xy}^2} \\
i_{uy} = \frac{p \cdot v_{uy} - q \cdot v_{ux}}{v_{xx}^2 + v_{xy}^2}
\]  

For the next control step \((k+1)\) the dual converter voltage needed for impressing system current defining the required active and reactive power flow is given by the following expressions [15].

\[
\bar{v}_s(k+1) = \bar{v}_s(k+1) - \frac{L_{AF}}{T_s} \left[ \bar{v}_s(k+1) - \bar{v}_s(k) \right] - R_{AF}\bar{i}_s(k)
\]  

An approximate value of \(\bar{v}_s(k+1)\) can be obtained by rotating \(\bar{v}_s(k)\) by \(e^{j\omega T_s}\).

III. GENERALIZED SPACE VECTOR PWM METHOD

The dual converter’s space vector, \(\bar{v}_s\), is obtained using a generalized space vector modulation algorithm on each sub converter. This algorithm uses the following intermediate variables,

\[
f_x = v_{ux}; \quad f_y = \frac{v_{uy}}{\sqrt{3}}
\]  

Using these variables, a sector selector \(N(f_x, f_y)\) can be defined as

\[
N(f_x, f_y) = \left[ \frac{3\theta}{\pi} \right] = \
= 2.5 - \text{sgn}(f_y) [(f_x > f_y) + (f_x > -f_y) + 0.5]
\]  

In two level three phase converters the null vector can be obtained using states \((0,0,0)\) or \((1,1,1)\), and the amount of time employed to synthesize vector zero using either \((0,0,0)\) or \((1,1,1)\) is defined by \(\delta\); if \(\delta = 0\) the null vector is synthesized using only state \((1,1,1)\) and if \(\delta = 1\) the null vector is obtained using only \((0,0,0)\). For the modulation, a sector selector \(N(f_x, f_y)\) locates the space vector to be synthesized in one of the sectors in the hexagonal space, and defines the expressions needed for computing the required duty cycles \(D_a, D_b\) and \(D_c\), according to Table I. In Table I, \(\delta\) is used to select the modulation method.

<table>
<thead>
<tr>
<th>(N)</th>
<th>(D_a)</th>
<th>(D_b)</th>
<th>(D_c)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>(\delta (f_x + f_y - 1) + 1)</td>
<td>(D_a - f_x + f_y)</td>
<td>(D_a - f_x - f_y)</td>
</tr>
<tr>
<td>1</td>
<td>(D_a + f_x - f_y)</td>
<td>(\delta (2f_y - f_x - 1) + 1)</td>
<td>(D_a - 2f_y)</td>
</tr>
<tr>
<td>2</td>
<td>(D_a + f_x - f_y)</td>
<td>(\delta (-f_x + f_y - 1) + 1)</td>
<td>(D_a - 2f_x)</td>
</tr>
<tr>
<td>3</td>
<td>(D_a + f_x + f_y)</td>
<td>(D_a + 2f_y)</td>
<td>(\delta (-f_x - f_y - 1) + 1)</td>
</tr>
<tr>
<td>4</td>
<td>(\delta (f_x - f_y - 1) + 1)</td>
<td>(D_a - f_x + f_y)</td>
<td>(D_a - f_x - f_y)</td>
</tr>
</tbody>
</table>

Table I can be used directly as the algorithm for implementing the generalized SVPWM as a function of the null vector ratio \(\delta\). Table II shows the values of \(\delta\) required to implement several commonly used modulation methods.

<table>
<thead>
<tr>
<th>Modulation</th>
<th>(\delta)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DPWM_{main}</td>
<td>1</td>
</tr>
<tr>
<td>DPWM_{sense}</td>
<td>0</td>
</tr>
<tr>
<td>SVPWM</td>
<td>(\frac{1}{2})</td>
</tr>
<tr>
<td>DPWM_0</td>
<td>(\frac{1}{2} [1 + (-1)^{n_1}])</td>
</tr>
<tr>
<td>DPWM_1</td>
<td>(\frac{1}{2} [1 + (-1)^{n_2}])</td>
</tr>
<tr>
<td>DPWM_2</td>
<td>(\frac{1}{2} [1 + (-1)^{n_1 + 1}])</td>
</tr>
<tr>
<td>DPWM_3</td>
<td>(\frac{1}{2} [1 + (-1)^{n_2 + 1}])</td>
</tr>
</tbody>
</table>

For \((x, y)\) coordinates:

\(n_1 = N = 2.5 - \text{sgn}(f_y) [(f_x > f_y) + (f_x > -f_y) + 0.5]\)
\(n_2 = 3.5 - \text{sgn}(f_y + 3f_x) [(f_x > 0) + (f_x > 3f_y) + 0.5]\)

IV. GENERALIZED PRINCIPLE OF ALTERNATE SUB-HEXAGONAL CENTER

In a dual converter, space vectors can be synthesized using an infinite number of switching strategies for both sub converters. This plethora of combinations makes possible the
imposition of different constrains on the dual converter’s operation. For example, in the selection of a modulation strategy with reduced number of commutations, power flow regulation is done by controlling each sub converter contribution in the synthesis of the final space vector [3], [17], allowing for DC link voltage regulation. Additionally, different modulation methods can be used in each sub converter and a constraint on thermal stress on the power devices or common mode voltage reduction can be implemented.

In this work, a generalization of the alternate sub-hexagonal center PWM presented in [3], [16] is proposed. The duty cycle demands in each sub converter are computed by first selecting the modulation method from Table II, with the proper selection of $\delta$. With the modulation method selected, general 2-level duty cycles are computed and a “sub converter clamping selector” (SCCS) value is computed using the following expression,

$$SCCS = (D_a > 0.5) + (D_b > 0.5) + (D_c > 0.5) \quad (8)$$

For reducing the common mode voltage sub converter 1 is clamped if $SCCS < 2$ otherwise sub converter 2 is the one clamped [16]. If sub converter 2 is clamped, a further reduction in the common mode voltage can be achieved by employing $DPWM_{min}$ in sub converter 1. On the other hand, if sub converter 1 is clamped the reduction in common mode voltage can be increased by using $DPWM_{max}$ in sub converter 2. Figure 2(a) shows an example of space vector synthesis for $\delta = 1$, with sub converter 2 clamped and sub converter 1 using PWM to synthesize the remaining part of the space vector. The base vector for sub converter 1 are marked as $\{a, b, c\}$, and for sub converter 2 as $\{a', b', c'\}$ and they are the clamping values allowed for each sub converter. Figure 2(b) shows the clamping zones for both sub converters when using the modulation methods presented in [18]. It is important to notice that a change in the definition of $SCCS$ could produce additional clamping zones patterns. A useful constraint that can be imposed in the modulation process is how the power flows into each sub converter. The contribution to the space vector provided by each sub converter can have a different magnitude, while the current flowing into each sub converter is the same. Therefore, some control of the active power going into each sub converter can be obtained [4].

V. SIMULATION AND EXPERIMENTAL RESULTS

The dual converter system was simulated using MATLAB-SIMULINK to verify operation of the dual converter operating as a controlled rectifier under direct power control. Additionally, the simulations allow to verify the effect of different modulation methods over the DC link voltage imbalance on both sub converters.

For the experimental test, the proposed algorithm was implemented on a custom build floating-point DSP-(ADSP-21369) based test rig shown in Fig. 3(a). The power stage in each sub converter uses six 50 A, 1200V insulated gate bipolar transistors (IGBTs) with a 2200 $\mu$F, 450 V capacitor in the dc link and the sampling and switching frequency was 10 kHz.

Fig. 3(b) shows that only two out of six converter branches are under PWM while the remaining are not switching at any given control cycle. This happens only for the discontinuous modulation methods. Also, the clamped sub converter is operating with only one of its branches in high state.

The effect of the modulation method on the sub converters DC link voltage was first simulated, and the results for the modulation methods presented in Table II are shown in Fig. 4. These simulations show that for balanced loads, for continuous SVM only $\delta = 0.5$ produces balanced outputs. For discontinuous SVM, only $DPWM_{min}$ and $DPWM_{max}$ produce imbalances with opposite effect on the DC link voltages. This feature can be exploited to attain some degree of power flow control while clamping one of the sub converters using an algorithm equivalent to the one presented in [4].

Figure 5 shows the system line voltage ($\bar{v}_s$), the voltage at the dual converter’s input ($\bar{v}_s'$) and the system current ($\bar{i}_s$) for unity power factor operation. Figure 6 shows the harmonic content of the supply current $\bar{i}_s$ when the dual converter is operating using DPWM$_1$ and the power demands are for unity power factor operation, the resulting THD obtained in this experiment is 3.4%. Figure 7 shows the experimental DC link voltage for two modulation methods, in Fig. 7(a) shows the DC-link voltage evolution in each sub converter for the DPWM$_{max}$ method, and Fig. 7(b) shows the corresponding results for SVM ($\delta = 0.5$). These results are in agreement with the simulations presented in Fig. 4. Small mismatches in the voltage levels are due to tolerance errors in parameter values for both sub converters.
Fig. 3. Experimental test-rig and example of gate signals for DPWM2.

Fig. 4. Results for effect of modulation method on the sub converters DC-link voltage (simulation).
VI. CONCLUSION

The dual converter’s topology has been tested as a controlled rectifier, for increased power conversion employing lower voltage switching devices. The algorithm used in the control of the dual converter was an optimized version of the direct power control (DPC). Also, a generalization of the principle of alternate sub-hexagonal center have been presented, with the generation of different clamping zone patterns for commonly used modulation methods. Simulations and experimental results show that different modulation strategies can be employed in the regulation of DC links in both sub converters. Some modulation strategies allow the converter to operate in a balanced or imbalanced fashion. Also, the flexibility of the modulation strategies result in a reduction on the number of simultaneous switchings in the sub converters. The $\frac{dv}{dt}$ is reduced by the increased number of levels generated by the dual converter topology.

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